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La principal motivación de la Editorial es recoger y difundir los conocimientos relevantes en ciencia y tecnología, llevándolos a los sectores de la comunidad que los requieren.

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TECNOLOGÍA en marcha

Contenidos

Presentation

Presentación

Esteban Arias-Méndez[1]

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1 IEEE LAEDC 2022. Instituto Tecnológico de Costa Rica. EDS Costa Rica

On behalf of the organizing committee of IEEE Latin American Electron Devices Conference (LAEDC) 2022 we would like to welcome you to this fourth edition, which has been planned and organized this year as a hybrid event.

LAEDC is the flagship conference for EDS in Region 9 and offers an enriching opportunity to learn about many of the fields related to Electron Devices and novel technologies with more than 115 technical presentations, including 3 keynote lectures, 26 invited speakers, 60 scientific papers, a free of charge MOS-AK workshop, 17 poster presentations, and 2 panel sessions in topics related to Humanitarian Technology, HAC, and Women in Engineering, WIE.

The Conference is growing with worldwide participation with presentations from many countries and with the full financial sponsorship of the IEEE Electron Devices Society (EDS). It is primarily geared for students as well as young researchers, with the main goal of bringing together specialists from all Electron Device related fields.

This special issue is focused on the short papers related to EDS topics presented at the conference.

We are sure that, thanks to your active participation and tangible contributions, it will significantly increase the value of the conference and motivate research groups and young students in the field of electronic devices.

A Dual Core Source/Drain GAA FinFET

Un FinFET GAA de fuente/drenaje de doble núcleo

Prachuryya Subash Das[1], Deepjyoti Deb[2], Rupam Goswami[3], Santanu Sharma[4], Rajesh Saha[5], Hirakjyoti Choudhury[6]

Das, P.S; Deb, D; Goswami, R; Sharma, S; Saha, R; Choudhury, H. A dual core source/drain gaa finfet. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 5-11.

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Keywords

FinFET; Gate-all-Around; Dual Core; Interface Traps; Ribbon FET.

Abstract

The emergence of fin-shaped field effect transistors (FinFETs) was governed by the requirement of the VLSI industry to include more functionalities per unit chip area. Enhanced gate control in a FinFET due to a surrounding gate architecture built on the fundamental geometry of a MOSFET made them highly compatible to the existing CMOS circuit applications. The announcement of a vertically stacked multiple FinFET structure named as Ribbon-FET by Intel Corporation in 2021 motivates the work presented in this article. This article proposes a dual core source-drain gate-all-around FinFET, and evaluates its performance in terms of variation in core doping concentrations through technology computer aided design (TCAD) simulations. The advantage of having a dual core in source and drain regions is the opportunity to tune the performance metrics of the device by altering the doping concentration in the outer, and inner cores. The response of the optimized architecture to presence of acceptor-like, and donor-like traps in oxide/ channel interface is presented. The acceptor-like traps affect the characteristics in its on-state, whereas the donor-like traps influence the off-state of the device. DIBL reduces with the introduction of interface traps.

Palabras clave

FinFET; Puerta todo alrededor; Doble núcleo; trampas de interfaz; Ribbon FET.

Resumen

La aparición de transistores de efecto de campo en forma de aleta (FinFET) se rigió por el requisito de la industria VLSI de incluir más funcionalidades por unidad de área de chip. El control de puerta mejorado en un FinFET debido a una arquitectura de puerta circundante construida sobre la geometría fundamental de un MOSFET los hizo altamente compatibles con las aplicaciones de circuitos CMOS existentes. El anuncio de una estructura FinFET múltiple apilada verticalmente denominada Ribbon-FET por Intel Corporation en 2021 motiva el trabajo presentado en este artículo. Este artículo propone un FinFET completo de puerta de drenaje de fuente de doble núcleo y evalúa su rendimiento en términos de variación en las concentraciones de dopaje del núcleo a través de simulaciones de tecnología de diseño asistido por computadora (TCAD). La ventaja de tener un núcleo doble en las regiones de origen y drenaje es la oportunidad de ajustar las métricas de rendimiento del dispositivo alterando la concentración de dopaje en los núcleos externo e interno. Se presenta la respuesta de la arquitectura optimizada a la presencia de trampas de tipo aceptor y de tipo donante en la interfaz óxido/canal. Las trampas de tipo aceptor afectan las características en su estado activado, mientras que las trampas de tipo donante influyen en el estado desactivado del dispositivo. DIBL se reduce con la introducción de trampas de interfaz.

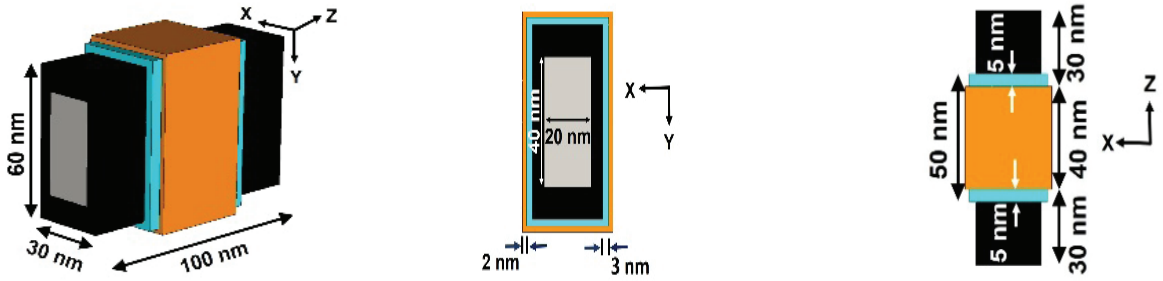
Introduction

The improved gate control on channel by transforming the body of planar metal oxide semiconductor field-effect transistors (MOSFETs) into a fin-shaped geometry has made FinFETs one of the quickest architectures to have a research-to-market translation [1]. The orientation of the semiconductor device industry towards ribbon-FET architectures or multi-level vertically stacked gate-all-around (GAA) structures to address efficient power management has created

the need for evaluating architectures with more control parameters [2]. This article proposes a dual core (DC) GAA FinFET with dual doping concentration in its source, and drain regions, and examines it for variation in doping concentration, and presence of interface traps through technology computer-aided design (TCAD) simulations.

Device architecture and simulation set-up

The schematic of the DC GAA FinFET is shown in Fig. 1 (a)-(c), where the source, and drain regions have dual cores (outer core doping: OC, inner core doping: IC), and the channel region is a solo core structure with a doping concentration of $10^{17}cm^{-3}$. Such a geometry offers the option to modulate the electrical characteristics of the proposed architecture through change in doping concentrations. Calibrated simulations have been carried out on Sentaurus TCAD tool (Synopsys Inc.) [3] in accordance with the parameters as mentioned in the article, [4].



(a) (b) (c)

Figure 1. (a) 3D view; (b) Front view; (c) Top view of the DCGAA FinFET.

Results and discussion

The effect of variation in dual core doping concentration on transfer characteristics of the proposed device with SiO_2 as a gate oxide (GOx) is shown in Fig. 2 (a). The presence of bandgap narrowing model (BGN) slightly decreases the drain current as shown in the inset due to the change in energy bandgap in regions of high doping. Therefore, the barrier height increases for carriers in source/ channel junction as evident from the conduction band edge profile in Fig. 2 (b), plotted along the source-channel-drain position (*z*-axis) at $x = W/2$, $y = H/2$ (*W*: fin width, *H:* fin height) at V_{GS} = 0.1 V. As evident from Fig. 2 (a), and Table 1, $OC = IC = 10^{19}cm^{-3}$ offer the highest on-state current I_{ON} , yet, it offers a lower switching current ratio (I_{ON}/ I_{OFF}). On the contrary, $OC = IC = 10^{18}\ cm^{-3}$ offer the best off-state current (I_{OFF}), threshold voltage (V_{TH}), and subthreshold swing (*SS*). A further insight into the absolute electric field profiles along the *z*-axis at $x = W/2$, $y = H/2$ for all the four cases of doping concentrations in Fig. 2 (c) in on-state shows the maximum peak for $OC = IC = 10^{19}\ cm^{-3}$, and the minimum peak for $OC = IC = 10^{18}\ cm^{-3}$.

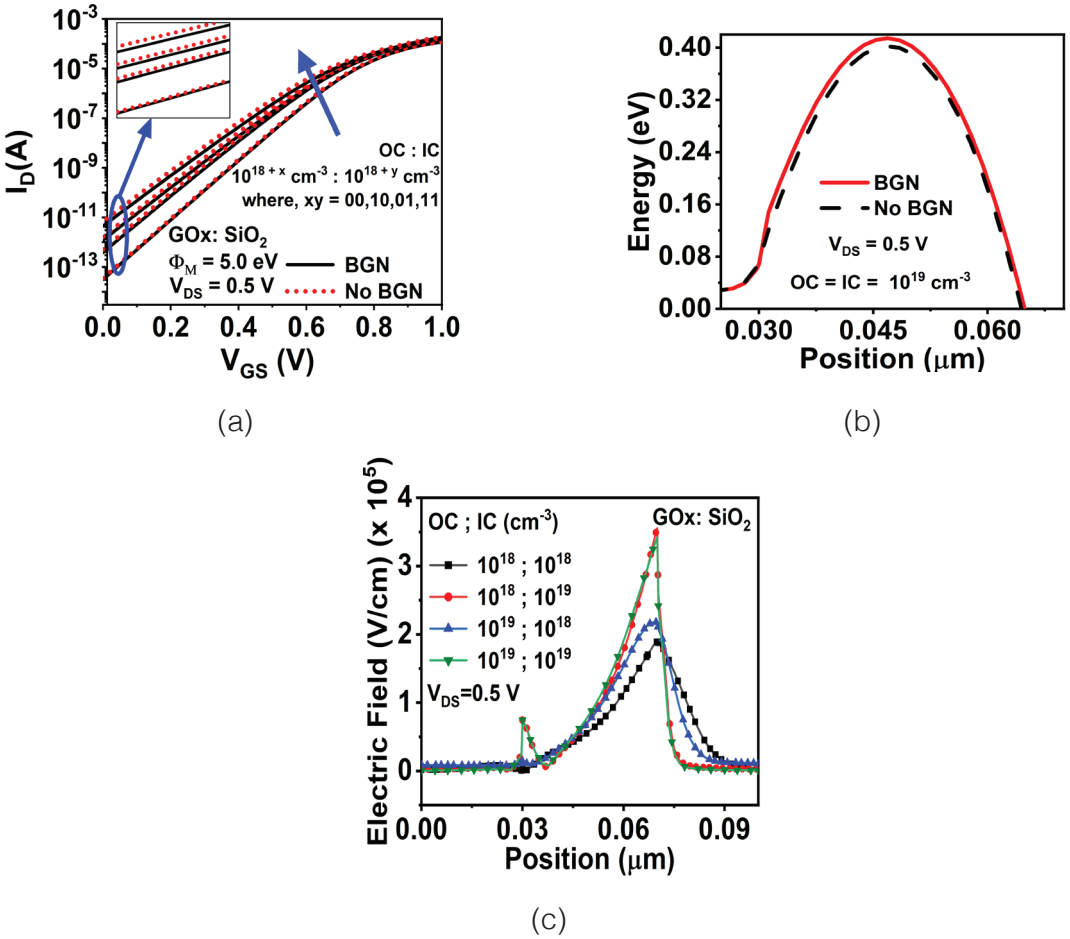


Figure 2. (a) Transfer characteristics of DC GAA FinFET for different outer core (OC), and inner core (IC) doping concentrations with and without bandgap narrowing effects; (b) Conduction band energy with and without BGN in the channel along z-axis at $x = W/2$, $y = H/2$ $V_{GS} = 0.1V$; (c) Absolute electric field profiles along z-axis at $x = W/2$, $y = H/2$.

Table 1. Electrical characteristics of DC GAA FinFET for different core doping concentrations without BGN [Fig. 2 (a)]

Outer Core Doping (cm^{-3})	Inner Core Doping (cm^{-3})	I_{ON} (μA)	I_{OFF} (ρA)	I_{ON}/I_{OFF} (x 10^7)	V_{TH} (V)	Subthreshold Swing (mV/dec)
10^{18}	10^{18}	118.833	0.031	378.6	0.777	84.123
10^{18}	10^{19}	154.151	1.200	12.83	0.778	96.654
10^{19}	10^{18}	165.869	0.385	43.02	0.791	87.499
10^{19}	10^{19}	179.678	4.476	4.013	0.781	99.600

To consider an optimized set of electrical characteristics with priority on I_{ON}, and I_{ON}/I_{OFF}, the architecture with $OC = 10^{19}\ cm^{-3}$, and $IC = 10^{18}\ cm^{-3}$ is considered for further observations, taking HfO_2 as gate oxide (GOx). Figure 3 (a) compares the transfer characteristics of the optimized architecture in the absence, and presence of trap states (acceptor-like traps, and donor-like traps) at the gate-oxide/ channel interface. The trap distribution is considered to be Gaussian, and defined in the TCAD tool as,

$$D_{GAU} = N_0 exp\left|{(E - E_0)^2}/{2E_S^2}\right| \quad (1)$$

where, N_0 = 10^{13} cm^{-2}, E_0 = 0.55 eV from valence band edge, E_S = 0.1 eV [5].

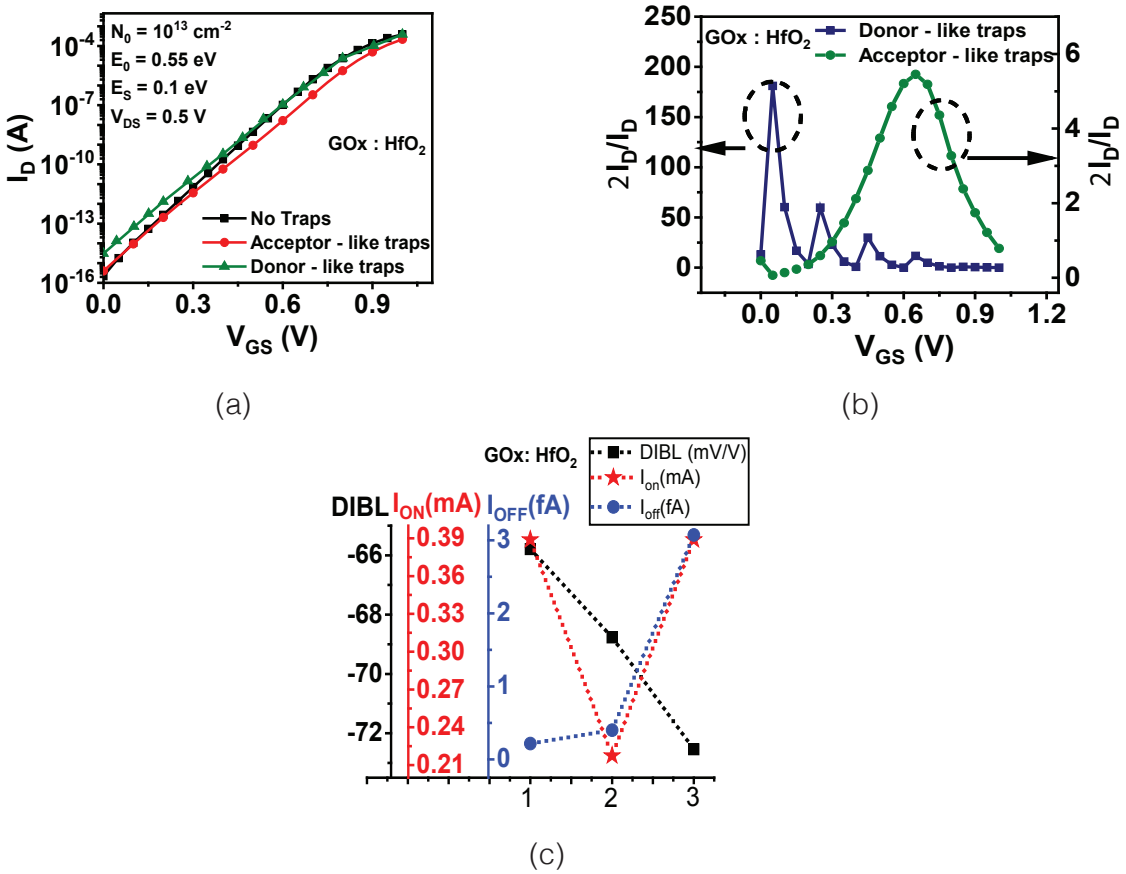


Figure 3. (a) Transfer characteristics of DC GAA FinFET for optimized doping concentrations in presence, and absence of oxide/channel interface traps having Gaussian distribution, peaked at 0.55 eV, and standard deviation of 0.1 eV; (b) Trap sensitivity for the transfer characteristics in (a); (c) Comparison plots of DIBL, I_{OFF}, and I_{ON} for no traps (Sl. 1), acceptor-like traps (Sl. 2), and donor-like traps (Sl. 3)

It is observed that the transfer characteristics in absence of traps overlaps with the characteristics for acceptor-like traps in off-state, and overlaps with the characteristics for donor-like traps in on-state. The comparison becomes more prominent when the trap sensitivity is plotted in Fig. 3 (b) in terms of $\Delta I_D/I_D$ where I_D is the drain current, taking the case for no traps as a reference [5]. The case for donor-like traps exhibits maximum peak in the low-V_{GS} region close to off-state, whereas for acceptor-like traps, the peak is exhibited in the mid-V_{GS} region in the on-state. Figure 3 (c) presents a multi-YYY plot for drain induced barrier lowering (DIBL), I_{OFF}, and I_{ON} for three cases: 1 (no traps), 2 (acceptor-like traps), and 3 (donor-like traps). The DIBL, measured using constant current method at I_D= 0.1 μA decreases as interface traps are introduced, which indicates that the trapping of carriers close to the interface is dominant enough to reduce the ΔV_{TH} difference at lower, and higher V_{DS}.

With reference to the inference from Fig. 3 (b), electrostatic potential profiles are plotted for acceptor-like traps (on-state, V_{GS} = 0.9V), and donor-like traps (off-state, V_{GS} = 0.0V) in Fig. 4 (a) and Fig. 4 (b) by comparing with corresponding profiles for no traps at respective V_{GS}, showing the region(s) of influence where the variation is observed.

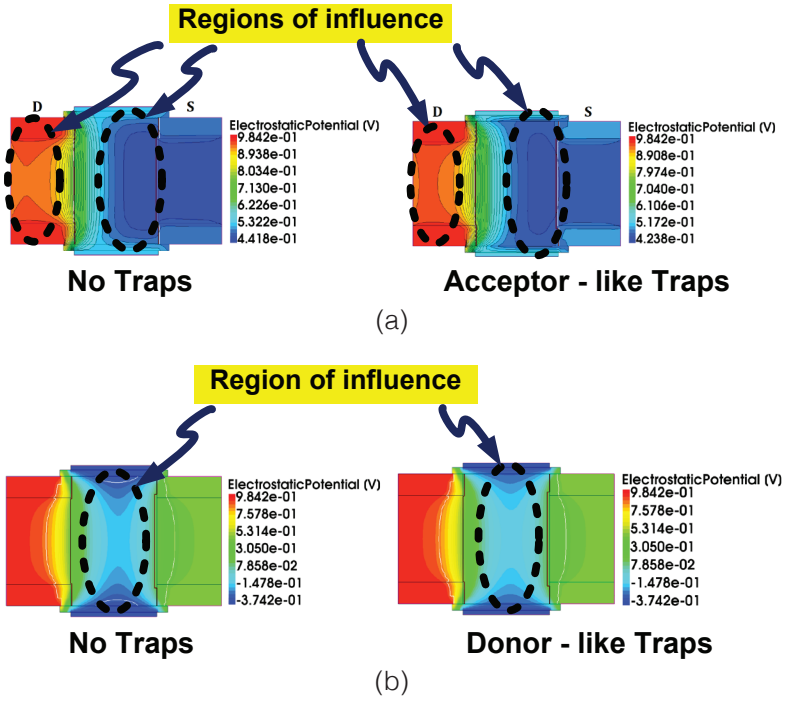


Figure 4. Electrostatic potentials along z-axis at $x = w/2$ for (a) acceptor-like traps at $V_{GS} = 0.9V$, and (b) donor-like traps at $V_{GS} = 0.0V$ by comparing with corresponding profiles for no traps in respective V_{GS}.

Conclusion

This article proposed a geometry of a dual core source/ drain FinFET, and reported its performance in absence, and presence of interface traps. The conclusions of the article can be summed up as follows.

- Modulation of electrical parameters is possible by tuning the doping concentrations in the two cores.
- Donor-like interface traps are dominant in off-state, whereas acceptor-like interface traps are dominant in on-state. The parameter, interface trap sensitivity, reveals this nature.
- DIBL reduces with the introduction of interface traps.

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A Dual Core Source/Drain GAA FinFET

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ABSTRACT

This article proposes a dual core source-drain gate-all-around FinFET, and evaluates its performance in terms of variation in core doping concentrations through technology computer aided design (TCAD) simulations. The response of the optimized architecture to presence of acceptor-like, and donor-like traps in oxide/ channel interface is presented. The acceptor-like traps affect the characteristics in its on-state, whereas the donor-like traps influence the off-state of the device.

INTRODUCTION

FinFETs are one of the fastest architectures to go from research to market. They have increased gate control on channel by converting the body of planar MOSFETs into fin-shaped geometry[1]. To solve effective power management, the semiconductor device industry has shifted its focus toward ribbon-FET architectures or multi-level vertically stacked gate-all-around (GAA) structures. Intel introduces vertical stacking of GAA FinFETs (named as Ribbon FET) in 2021[2].

DEVICE ARCHITECTURE AND SIMULATION SET-UP

The schematic of the DC GAA FinFET is shown in Fig. 1 (a)-(c), where the source, and drain regions have dual cores (outer core doping: OC, inner core doping: IC), and the channel region is a solo core structure with a doping concentration of $10^{17}cm^{-3}$. Such a geometry offers the option to modulate the electrical characteristics of the proposed architecture through change in doping. Calibrated simulations have been carried out on Sentaurus TCAD tool (Synopsys Inc.) in accordance with the parameters as mentioned in [3][4].

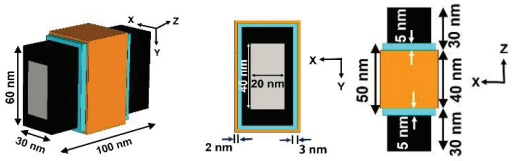

Figure 1: (a) 3D view; **(b)** Front view; **(c)** Top view of Dual Core (DC) GAA FinFET

RESULTS AND DISCUSSION

Table 1. Electrical characteristics of DC GAA FinFET for different core doping concentrations without BGN [Figure 2]

Outer Core Doping (cm^{-3})	Inner Core Doping (cm^{-3})	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF} ($\times 10^7$)	V_{TH} (V)	Subthreshold Swing (mV/dec)
10^{18}	10^{18}	118.833	0.031	378.6	0.777	84.123
10^{18}	10^{19}	154.151	1.200	12.83	0.778	96.654
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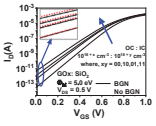


Figure 2

- As evident from Figure 1 (d), and Table 1, $OC = IC = 10^{19}cm^{-3}$ offer the highest on-state current (I_{ON}), yet, it offers a lower switching current ratio (I_{ON}/I_{OFF}).
- $OC = IC = 10^{18}cm^{-3}$ offer the best off-state current (I_{OFF}), threshold voltage (V_{TH}), and subthreshold swing (SS).

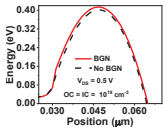


Figure 3

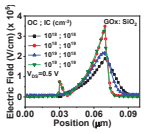
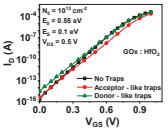


Figure 4

- The presence of bandgap narrowing model (BGN) slightly decreases the drain current as shown in the inset due to the change in energy bandgap in regions of high doping[Figure 3].
- The absolute electric field profiles along the z-axis at $x = W/2,\ y = H/2$ for all the four cases of doping concentrations in on-state shows in Figure 4.



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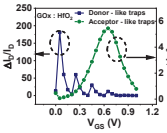

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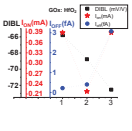

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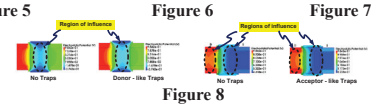

Figure 8

- The transfer characteristic shown in Figure 5 for no traps overlaps with the characteristic for acceptor-like traps in off-state, and overlaps with the characteristic for donor-like traps in on-state[5].
- Donor-like traps exhibits maximum peak in the low-V_{GS} region close to off-state[Figure 6].
- Acceptor-like traps, the peak is exhibited in the mid-V_{GS} region in the on-state [Figure 6].
- The DIBL, measured using constant current method at $I_D = 0.1\ \mu A$ decreases as interface traps are introduced [Figure 7].
- Indicates that the trapping of carriers close to the interface is dominant enough to reduce the ΔV_{TH} difference at lower, and higher V_{DS}.

CONCLUSION

- Modulation of electrical parameters is possible by tuning the doping concentrations in the two cores.
- Donor-like interface traps are dominant in off-state, whereas acceptor-like interface traps are dominant in on-state.
- DIBL reduces with the introduction of interface traps.

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2022 IEEE Latin American Electron Devices Conference (LAEDC)

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Illustration 1. Presented poster at LAEDC 2022.

A pathway to In-Memory Computing driven Wellness Digital Twin utilizing Remote Patient Monitoring System (WDT-RPMS)

Un camino hacia un Gemelo digital de bienestar impulsado por la computación en memoria utilizando el sistema de monitoreo remoto de pacientes (WDT-RPMS)

Kishore Kumar Kadari[1], Ali Shiri Sichani[2], Wilfrido Moreno[3]

Kadari, K.K; Sichani, A.S; Moreno, W. A pathway to in-memory computing driven wellness digital twin utilizing remote patient monitoring system (WDT-RPMS). *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 12-22.

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Keywords

Memristor; in-memory computing; MBSE; precision medicine; healthcare; Digital Twin.

Abstract

With fast-paced digital transformation, precision medicine has been an essential part to elevate the conscience of healthcare with respect to the biopsychosocial model with the help of Remote Patient Monitoring Systems. Digital twins have been successful in many industries, in healthcare, it can optimize the wellness of the human body to improve physical and mental wellness including the non-diagnosed diseased populations and rural populations.

In this paper, we discuss the challenges in terms of computing to implement a complex system called Wellness Digital Twin-based Remote Patient Monitoring System following Model-Based Systems Engineering (MBSE), we present the definition, needs of the digital twin in the context of wellness and healthcare, a feasibility study followed by a concept of operations. Subsequently, we present the requirements and architecture including In-memory computing, (Emerging Non-Volatile Memories, memristive devices) that will enhance sensing, analytics, and levers of action.

Palabras clave

Memristor; computación en memoria; MBSE; medicina de precisión; cuidado de la salud; gemelo digital.

Resumen

Con la rápida transformación digital, la medicina de precisión ha sido una parte esencial para elevar la conciencia de la atención médica con respecto al modelo biopsicosocial con la ayuda de sistemas de monitoreo remoto de pacientes. Los gemelos digitales han tenido éxito en muchas industrias, en la atención médica puede optimizar el bienestar del cuerpo humano para mejorar el bienestar físico y mental, incluidas las poblaciones enfermas no diagnosticadas y las poblaciones rurales.

En este artículo, discutimos los desafíos en términos de computación para implementar un sistema complejo llamado Wellness Digital Twin-based Remote Patient Monitoring. Siguiendo la Ingeniería de Sistemas Basada en Modelos, presentamos la definición y las necesidades del gemelo digital en el contexto del Bienestar y la atención médica, un estudio de viabilidad seguido de un concepto de operaciones. Posteriormente, presentamos los requisitos y la arquitectura, incluida la computación en memoria (memorias emergentes no volátiles, dispositivos memristivos) que mejorarán la detección, el análisis y las palancas de acción.

Introduction

Healthcare services are going through a digital transformation [1] due to increasing data, improving computing power, high-speed communication systems [2] and mobile connectivity technologies. A study in Europe [3] about the key barriers in the healthcare sector emphasized the necessity of remote patient monitoring and the Wellness Digital Twin (WDT).

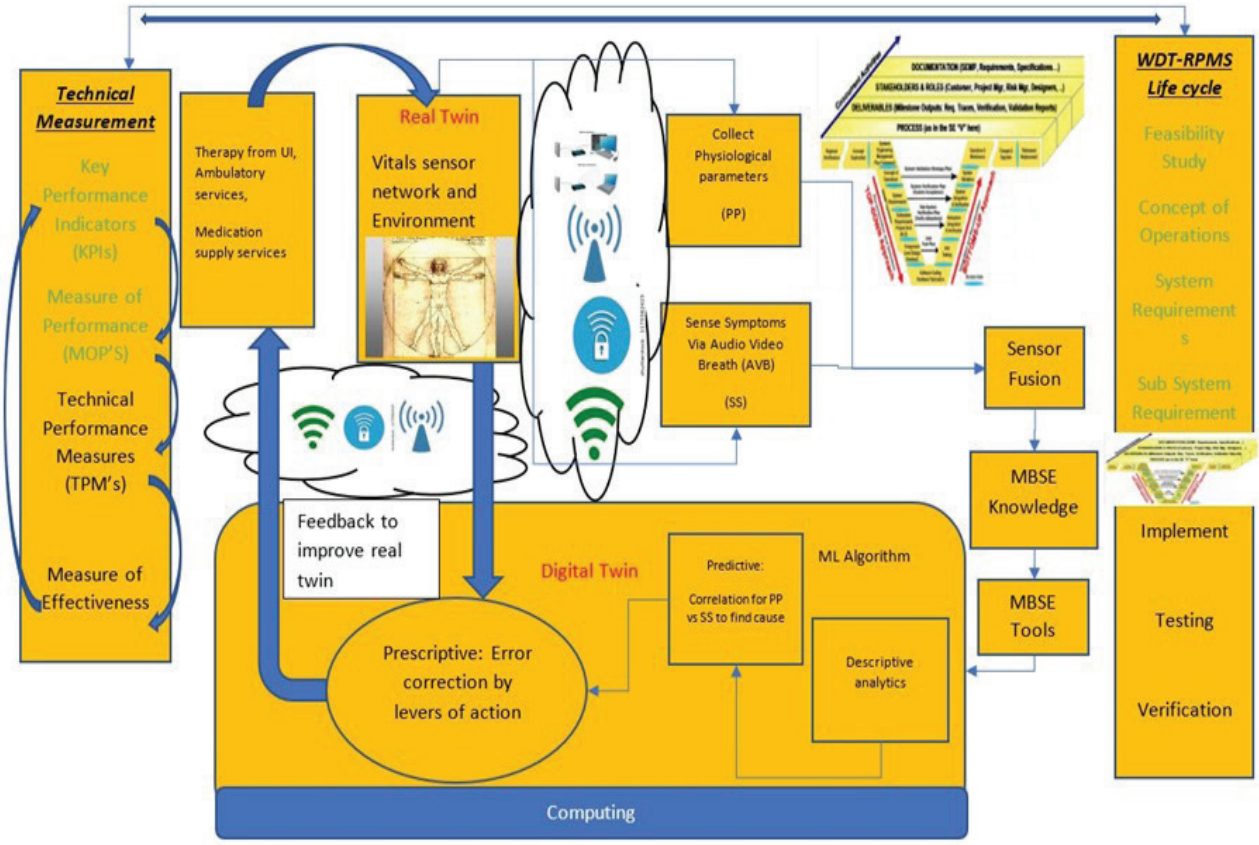

Figure 1. Wellness Digital Twin using Remote Patient Monitoring System.

Definition of Wellness Digital Twin (WDT)

1. Definition of Wellness Digital Twin (WDT): "Digital twins enable the monitoring, understanding, and optimization of all functioning of humans, and provide constant health insight to improve quality of life, and well-being" [4] From the above definition, the features from literature are data visualization, prediction, intelligence, analysis, decision making, and feedback loop [4]
2. Definition of Electronic Health: FDA states eHealth as a digital informational tool between healthcare and users, World Health Organization (WHO) states it as safe use of information and communication [3].
3. Definition of Remote Patient Monitoring Systems (RPMS): RPMS is a combination of organizational techniques, Electronic Health [3], engaging users using information and training [5].
4. Definition of Model-Based Systems Engineering (MBSE): MBSE is an integrated, consistent, coherent system modeling methodology that uses Systems Modeling Language (SysML), modeling methods, and modeling tools for the design, modeling, synthesis, and verification of complex systems.

In [5], the necessity of a systematic methodology for RPMS is well specified. The complexity of WDT-RPMS due to the great diversity of stakeholders requires the use of methodologies such as design thinking [6] and Model-Based System Engineering (MBSE) [7], [8] throughout the life

cycle. A system model captures design decisions as an element in a repository. The multiple elements are linked and stored in a database in the systems model. [8] An MBSE modeling tool, Magic System of Systems is used for the life cycle stages depicted in figure 1.

Feasibility study

About 80% of health spending in 2019 went towards care and treatment. 60% of spending is expected to be invested in improving health and well-being by 2040. [9] Consumers shall be empowered to monitor their health using technologies that can detect the initial stages of disease in asymptomatic people and convey drivers of health early which in turn help to prevent diseases. [4], [9]

Existing RPM services such as Extension for Community Healthcare Outcomes (ECHO) that deliver care for cancer [10], and hepatitis C virus treatment [11] played a key role in serving remote parts of New Mexico.

1. Business Plan: WDT-RPMS is a subscription-based model. The payment is of two types. The estimated selling price would be $150 (USD) for hardware with one year warranty. The estimated selling price for the subscription of the private consumer is $29 (USD) per month. The selling price for the subscription of Government consumers is $160 (USD) per month. Computer Vision is the current focus of the WDT-RPMS for patient pose monitoring to deliver its service in at least two years into the market.
2. Holistic approach to wellness: This research is focused on creating a holistic wellness-based system through digital twins using data acquired from real humans also called “real twins” [4]. The data creation, maintenance, and digital transformation are utilized to increase the positive outcomes for the real twin [12]. While healthcare monitoring is pervasive [3], [13], [14] and complex [12], the Wellness Digital Twin utilizes Remote Patient Monitoring Services (RPMS) and is referred to it as WDT-RPMS. WDT-RPMS network data is combined with Electronic Medical Records (EMR) and other datasets to reveal hidden insights into population health outcomes.
3. Advances in Computing: The technological advances in both communication (wireless communication services [2]) and computing research enable digital transformation. The existing computers have von Neumann architecture in which the computation and the memory are physically separated. The data is fetched from memory and transported to the processing unit, where computation happens, and then transported back to the memory unit for storage purposes. The transportation of data between the processing unit and memory costs performance as a memory wall and the high-power dissipation. [15] In-memory process using emerging Nonvolatile Memories (eNVM) specifically, memristive devices will accelerate computing rate with low energy consumption, and low latency.

Methods- Concept of Operations for WDT-RPMS

The main purpose of the WDT-RPMS system is to improve health outcomes for the patients which directly reduces the cost and improves the quality of health care. WDT-RPMS addresses the large undiagnosed diseased population. WDT-RPMS are designed to minimize Emergency room visits, hospital admissions, and re-admissions and to reduce overall healthcare costs.

RPMS-based WDT system remotely captures health information from users. Information is securely transmitted to the platform in the cloud. In addition, the system provides patient information to healthcare providers and authorized family members. The WDT has its own Artificially Intelligent robotic system to enable precision medicine using RPMS. The robotic

system sense and acts for monitoring the patients to help care providers to decrease the effects of chronic disease and to increase well-being with the help of descriptive analytics, predictive analytics, and prescriptive analytics.

The users of WDT-RPMS technology are doctors, patients, and caregivers. A sample of stakeholders for a WDT-RPMS are sales, marketing, medical support team, technical support team, development, and testing team.

Stakeholder needs:

Stakeholder's needs are collected from individual stakeholders as follows.

- To monitor vitals, which include blood pressure, glucose levels, body temperature, oxygen levels in the blood, body weight, and respiration rate. [16]
- To monitor the patient bedside pose using the camera. [17], [18]
- To monitor the breath contents and volatile organic compounds (VOC) information to diagnose pulmonary disorders, especially lung cancer the second most common cancer. [19]
- To collect the speech and respiratory symptoms using a microphone. [20]
- To perform real-time communication between patient information and doctor during alerts.
- To access historical patient data
- To provide secure data encryption during transmission and at rest for meeting Health Insurance Portability and Accountability Act (HIPAA).
- To meet Food and drug administration (FDA) compliance for home health devices.
- The ontology of the concept shows the flow of the operations sequentially in figure 2, but it could be more dynamic in real-time.

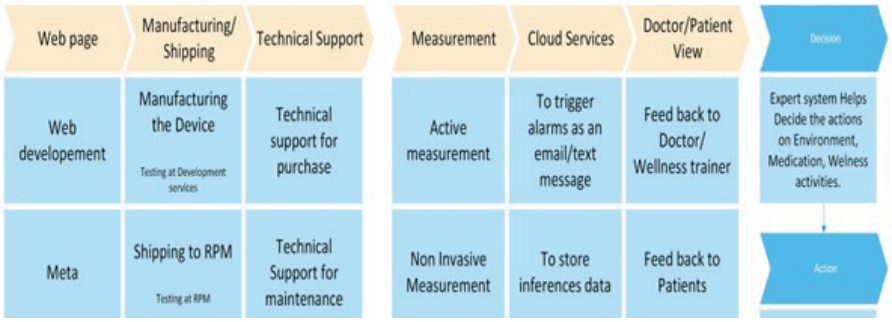

Figure 2. Operating Concept (OpsCon).

Opportunities and Challenges in Computing

Edge computing makes real-time inferences for large data sets using current advances in parallel computing. Internet of Things that are connected to Cloud-based computing can tune the machine learning-based models before deployment on the edge devices. The existing solutions are using parallelism through a Graphical Processing Unit (GPU) by utilizing multiple cores, each with the shared transportation connected with the memory. Another recent development is accelerators for specific applications, the Tensor Processing Unit (TPU) has been developed for the acceleration of Multiply-Accumulate (MAC) operation. Another progression is through elevating the memory bandwidth (the rate at which the data is transported while reading or

storing it back between processor and semiconductor memory) such as hybrid memory cube, and hybrid bandwidth memory. The latest advancement that has come to overcome the memory wall (the transportation gap between the processing space and the storage space) is a Resistive switching device. [15] An efficient edge computing, video processing pipeline subsystem with low latency and power that can perform millions of complex concurrent arithmetic operations per second is required. With the recent advancements in Resistive switching devices, Resistive RAM (RRAM) has achieved an ultra-low switching power and compatibility in-process fabrication as Complementary Metal Oxide Semiconductor (CMOS).

Results: Requirements and High-level architecture

WDT-RPMS system's high-level architecture and the state machine behavior of WDT-RPMS is built using the Magic System of Systems Model-based Systems Engineering tool as shown in figure 3, figure 4.

We summarize the sub system's requirements for the next stages of developing WDT-RPMS. The WDT-RPMS consists of sensors that acquire the vitals data, a microcontroller that processes the data, and a communication module that transmits the data and/or inferences to the cloud. The interface from the microcontroller to the mobile applications shall be via Bluetooth. The Nordic part shall be used to transmit data from Bluetooth to display on an application. The WDT-based RPMS is discussed in detail in the following subsections.

Computing:

The WDT-RPMS shall use RRAM-based computing (currently prototyping on Raspberry pi 4B and/or NVIDIA Jetson Nano microcontrollers). The cost of the cooling system shall be reduced due to RRAM revitalizing the data centers by utilizing the RRAM-based Convolutional Neural Networks (CNN) system [21].

Sensing

Medical sensing Devices shall be used to monitor the patients using evolving technologies to decrease the bridge between the healthcare providers and the patients by availing appropriate information technology systems.

1. Environment sensing: The autonomous Artificial Intelligence (AI) agent shall be able to sense the Sensor Variables (SV) like temperature (thermometer), airflow level (fan ON and OFF cases), humidity, and dust particle density (from particle sensor). Environment sensing is important while sensing the vitals because it is also dependent on the environment a person is in.
2. Audio Sensing: The acoustic data (Sound Symptoms for disease) collected by the microphone (embedded in a watch or smartphone application) with respect to time and location (To keep track of the allergens) whenever required shall be sensed. The Agent shall be able to detect the oxygen quantity in the blood and pulse rate to monitor the dust allergens [20].
3. Video Sensing: It shall help monitor the user's pose for conditions such as Stroke, Arrhythmia, Pregnancy, COVID/Long COVID, Obstructive Sleep Apnea, Old-age patients, and kids. The sleep pose dataset shall be used to make a model for classifying a patient's pose in bed. The video latency shall be less than 130 milliseconds using the raspberry pi camera.

4. **Breath Sensing**: The volatile organic compounds shall be sensed through nasal and oral breath contents to monitor lungs and gut health, respectively. Breathing rate shall be monitored by the microphone when needed.
5. **Vital sensing**: The vital sensing shall sense the blood pressure, glucose levels, body temperature, oxygen levels, and body weight. [22]

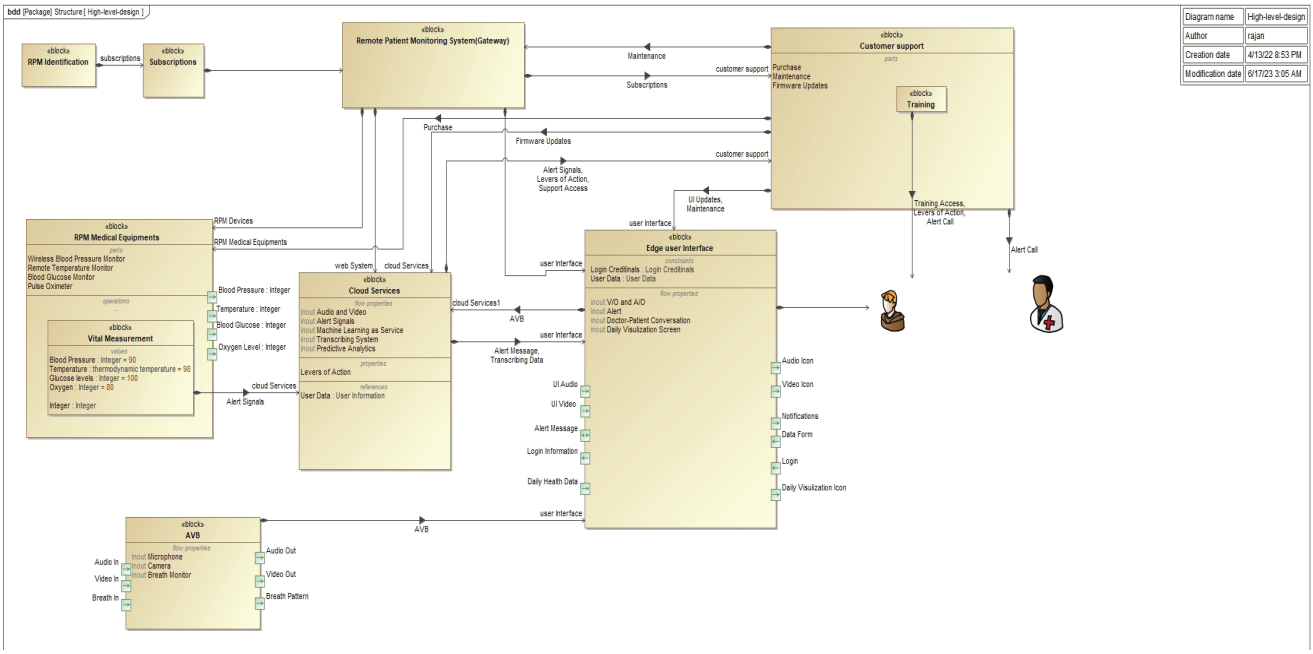

Figure 3. High-level Architecture.

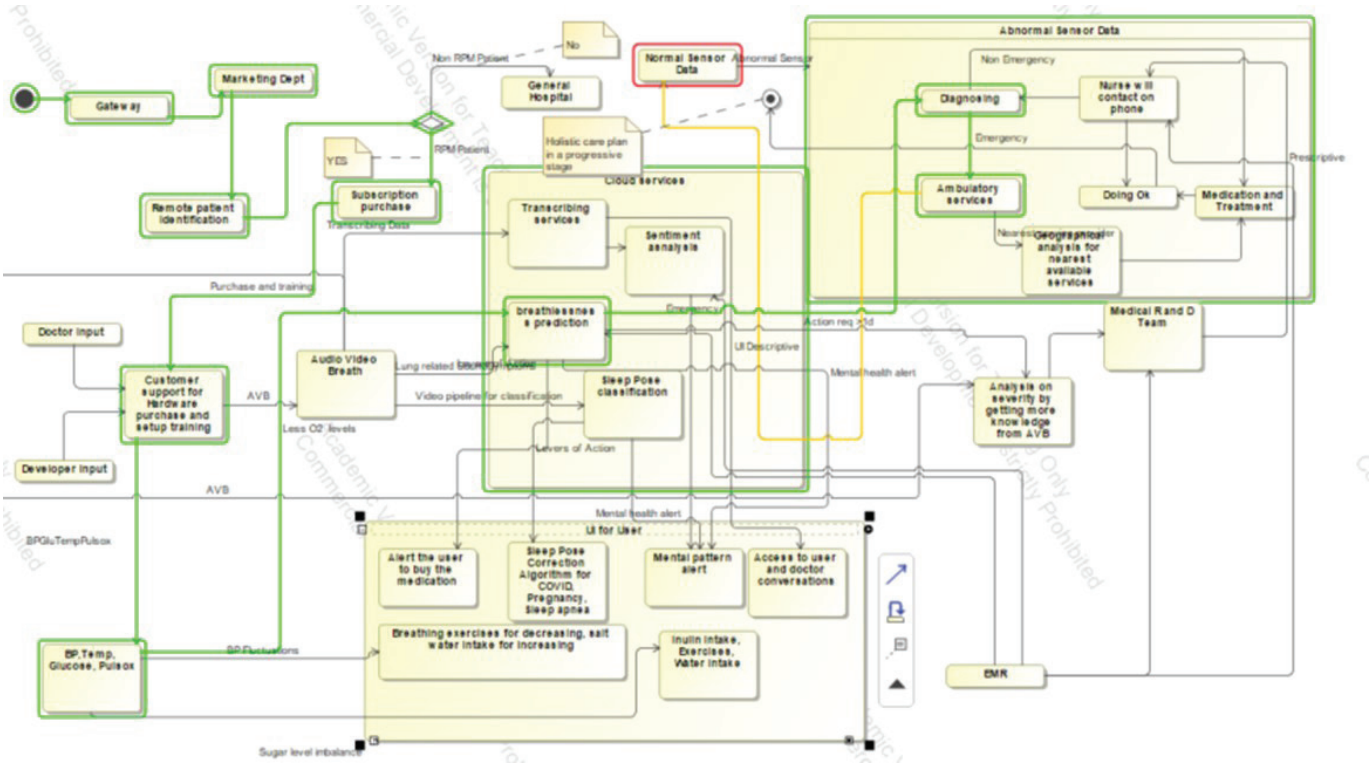

Figure 4. Simulation of State machine Behavior of the WDT-based RPMS.

Intelligence

1. Descriptive analytics: The sensors are used to convert the useful data in the form of text for further analytics. There are different forms of transcribing text from the given sensors.
    - Environment sensing to the text about the temperature, humidity, particle sensor readings, and GPS location.
    - Audio and Video to text from the time stamps and poses in that respective time stamps.
    - Breath sensor to text that shows the nature of the gut throughout the day.
    - Vitals to text to record the anomalies of the vitals.
2. Predictive analytics (Alerts): According to [23] the monitoring of vital signs can be the basis for the prediction of patient health status. Some of the different kinds of alerts discussed in the behavior of the system are
    - Alert user to buy medication for respective conditions
    - Breathlessness: Chronic Obstructive Pulmonary Disease (COPD) exacerbation alert, Corona Virus Disease (COVID) alert
    - Physiological: Blood Pressure (BP) fluctuations alert, Sugar level fluctuations alerts
    - Mental health alerts

To make the WDT-RPMS system efficient, constraints like genetic information, age, etc. shall be considered from Electronic Medical Records (EMR).

Levers of Action *(Prescriptions)*

1. To send an alert for Sleep pose correction based on scientific evidence. Levers of actions are shown with the problem against the solution below.
    - COVID/Long COVID Patient - to Prone position for better breathing. [24]
    - Pregnant women -to the left side to decrease stomach-related inconveniences [25]
    - Obstructive sleep apnea- Side-way sleeping [25]
2. To send an alert to do evidence-based breathing exercises
    - Slow and regular breathing can lower blood pressure (BP). [26]
    - Mental health: SKY breath reduces stress levels.[27], [28]

Conclusion

In-memory computing and MBSE make WDT-RPMS a reliable solution for precision medicine to improve individual health outcomes, thus it contributes to improving global health outcomes.

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LAEDC2022 LATIN AMERICAN ELECTRON DEVICES CONFERENCE

A Pathway to In-Memory Computing-driven Wellness Digital Twin utilizing Remote Patient Monitoring System (WDT-RPMS)

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Introduction

- Healthcare services are going through a digital transformation [1] due to increasing data, improving computing power, high-speed communication systems [2], and mobile connectivity technologies.
- A study in Europe [3] about the key barriers in the healthcare sector emphasized the necessity of remote patient monitoring and the Wellness Digital Twin (WDT).

Concept of Operations for WDT-RPMS

- RPMS-based WDT system remotely captures health information from users. Information is securely transmitted to the platform in the cloud.
- In addition, the system provides patient information to healthcare providers and authorized family members.
- The WDT has its own Artificially Intelligent robotic system to enable precision medicine using RPMS.
- The robotic system sense and acts for monitoring the patients to help care providers to decrease the effects of chronic disease with the help of descriptive analytics, predictive analytics, and prescriptive analytics.

WDT-RPMS Architecture

Requirements for WDT-RPMS

Computing: The WDT-RPMS shall use Resistive RAM In-Memory Computing which has ultra-low switching power.

Sensing:

- Environment sensing: The autonomous Artificial Intelligence (AI) agent shall be able to sense the Sensor Variables (SV) like temperature (thermometer), airflow level (fan ON and OFF cases), humidity, dust particle density (from particle sensor). Environment sensing is important while sensing the vitals because it also depends on a person's environment.
- Audio Sensing: The acoustic data (Sound Symptoms for disease) collected by the microphone (embedded in a watch or smartphone application [4]) with respect to time and location (To keep track of the allergens) whenever required shall be sensed.
- Video Sensing: It shall help monitor the user's pose for conditions such as Pregnancy, COVID/Long COVID, Obstructive Sleep Apnea, Old-age patients, and kids. The sleep pose dataset shall be used to make a model for classifying a patient's pose in bed.
- Breath Sensing: The volatile organic compounds shall be sensed through nasal and oral breath contents to monitor lungs and gut health, respectively. Breathing rate shall be monitored by the microphone when needed.
- Vital Sensing: The vital sensing shall sense the blood pressure, glucose, body temperature, oxygen, and body weight with respect to triggers of the disease.

Intelligence:

- Descriptive analytics: The sensors are used to convert the required data into the form of text for further analytics. There are different forms of transcribing text from the given sensors.
  - Environment sensing to the text about the temperature, humidity, particle sensor readings, GPS location.
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- Predictive analytics (Alerts): According to[5] the monitoring of vital signs can be the basis for the prediction of patient health status. The different kinds of alerts discussed in the behavior of the system are
  - Alert user to buy medication for respective conditions
  - Breathlessness: COPD exacerbation alert, COVID alert
  - Mental Health Alerts
  - To make the WDT-RPMS system efficient, constraints like genetic information, age, etc. shall be considered from Electronic Medical Records (EMR).
- Levers of Action (Prescriptive Analytics):
  - To send an alert for Sleep pose correction using wedges on the bed based on scientific evidence. Levers of actions are shown with the problem against the solution below.
    - COVID/Long COVID Patient - to Prone position for better breathing. [6]
    - Pregnant women -to the left side to decrease stomach-related inconveniences. [7]
    - Obstructive sleep apnea- Side-way sleeping.[7]
  - To send an alert to do evidence-based breathing exercises
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Illustration 1. Presented poster at LAEDC 2022.

Degradation indicators for power electronic converters

Indicadores de degradación para convertidores electrónicos de potencia

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Keywords

Fault; power converter; indicator; capacitor; switching transistor.

Abstract

Power electronic converters are an important element in the interaction between source and load. In fact, failures in this system often lead to bigger problems. Therefore, it is necessary to monitor the converter components that have the most failures. In this work, we present the estimation of three parameters, which are, in turn, degradation indicators of components in the power electronic converters: equivalent series resistance, capacitance and on-state resistance. Using current and voltage measurements of the Boost converter.

Palabras clave

Falla; convertidor de potencia; indicador; capacitor; transistor de conmutación.

Resumen

Los convertidores electrónicos de potencia son un elemento importante en la interacción entre la fuente y la carga. De hecho, los fallos en estos sistemas a menudo conducen a problemas mayores. Por lo tanto, es necesario monitorear los componentes del convertidor que tienen más fallas. En este trabajo presentamos la estimación de tres parámetros, que son a su vez indicadores de degradación de componentes en los convertidores electrónicos de potencia: resistencia equivalente serie, capacitancia y resistencia de encendido; usando medidas de corriente y voltaje del convertidor Boost.

Introduction

Given the importance of continuous and correct operation of power electronic converters (PECs), which are an essential part of more complex systems [1] In fact, PECs have the function of direct interaction between generation and load, besides, the control strategies or maximum power point tracking (MPPT), as with microgrids or PV systems [2].

According to [3], static PECs have component failures of 60% in capacitors, 30% in switching transistor, and 10% in inductors and diodes. Therefore, it is necessary to know the state-of-health (SOH) of the PEC main components for the correct operation of the system. Indeed, some component parameters, such as capacitance (C), equivalent series resistance (ESR) of a capacitor, and on-state resistance ($R_{ds,on}$) in MOSFETs, are indicators of degradation. This article seeks to contribute to establishing the main degradation indicators of electrolytic capacitor and switching transistor in a PEC. In section II, electronic component parameters that can be used as indicators of degradation are shown. Estimation of degradation indicators of the PECs is presented in section III. Finally, the expected results are shown.

Indicators of degradation

Since the capacitor and switching transistor of static PECs have the highest failure rate, some degradation indicators used will be shown. Electrical parameters, such as C, ESR, and physical parameters, such as volume, can show degradation [4]. In the case of MOSFETs, ($R_{ds,on}$), drain-source voltage ($V_{ds,on}$), and junction temperature are some indicators of degradation

[5]. However, the measurement of electrical parameters has the advantage of using sensors already available in the systems. Table 1 summary shows some degradation fault limits for the electrolytic capacitor and MOSFET.

Table 1 Degradation fault limits.

Parameter	Limit
ESR	*Increase of twice the nominal value*
C	Decrease to 80% the nominal value
$R_{ds,on}$	Increase to 25% of the nominal value

Estimation of degradation indicators of the PECs

To establish the degradation indicators of *ESR, C*, and $R_{ds,on}$, a Boost converter is used, as shown in Figure 1.

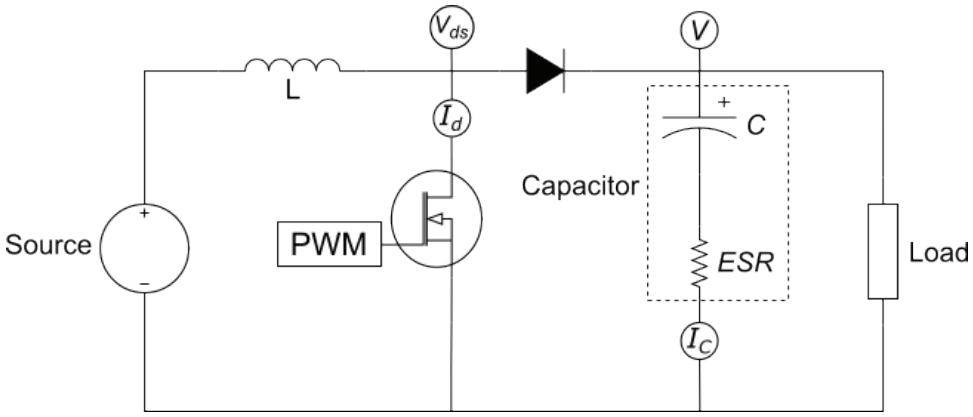

Figure 1. Boost converter.

Table 2 lists Boost converter parameters [6], which corresponds to the experimental setup available in the test microgrid developed at *Laboratorio de Accionamientos Eléctricos y Electrónica de Potencia at Universidad del Valle-Colombia.*

Table 2 Boost converter parameters.

Parameter	Variable	Value	Units
Switching frequency of Boost	F_{SW}	*20*	*kHz*
Inductor	*L*	5	*mH*
Output capacitor	*C*	2200	*mF*
Equivalent series resistance	*ESR*	114.5	*mΩ*
On-state Resistance	$R_{ds,on}$	70	*mΩ*

Capacitor

There are two classical representations of capacitor degradation estimation using *ESR* in PECs: ohmic frequency range and power losses of the capacitor.

The first technique, developed by [7], evaluates voltage/current signals within the ohmic frequency range of capacitors. It requires a band-pass filter (see Figure 2). Where V and I_C are capacitor voltage and current values (RMS), respectively. It is also necessary to adjust the gain for the input signal range in the processor that is calculating the *ESR*.

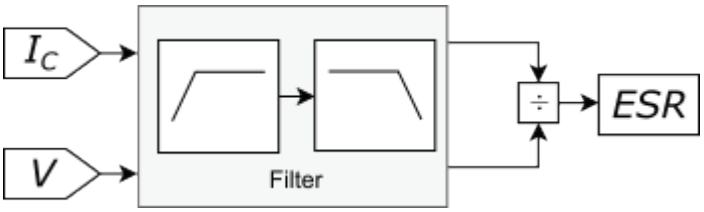

Figure 2. Technique of ohmic frequency range.

The second technique is proposed by [8], which avoids extensive filtering by calculating the AC power losses of the capacitor. Therefore, the *ESR* can be estimated as shown in the Figure 3. It also used the Rogowski coil to measure the capacitor current.

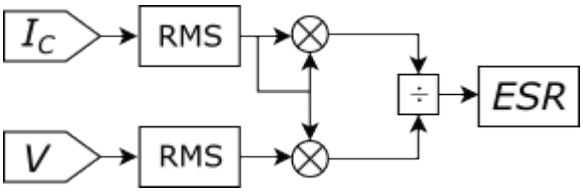

Figure 3. Technique for AC power losses.

However, it is necessary the estimation of both parameters of the capacitor for establishing its degradation. For example, in previous work [2], a grid-connected photovoltaic system, both parameters, *C* and *ESR*, of a DC-link capacitor were estimated using an electrochemical impedance spectroscopy (EIS) method.

Estimation errors in Matlab/Simulink using three techniques present, are 0.087%, 0.026% only ESR. In addition, the last technique for the parameters *ESR* and *C* are 0.53% and 0.37%, respectively.

Switching transistor: MOSFET

In this approach, it needs to measure the drain-source voltage ($V_{ds,PWM\text{-}on}$) and drain current ($I_{d,PWM\text{-}on}$), then $R_{ds,on}$ is calculated, as shown in Figure 4, However, a disadvantage of this method is that it requires high sampling, since the measurement values of interest are when the MOSFET is active. Estimation error of $R_{ds,on}$ in Matlab/Simulink using the procedure shown above, is 4.28%.

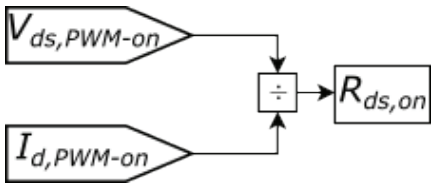

Figure 4. Estimation of on-state resistance of the switching transistor.

The next steps for this research are described below. Initially, in the setup experimental, measure the capacitor current and output voltage to get and compare the *ESR* with the methods presented. Likewise, a control strategy will be implemented. Then, the estimated values will be used in fault diagnosis. With MOSFETs, other degradation indicators will be evaluated using available measurements in the PECs.

Conclusions

This study shows some different methods to establish PEC parameters, which in turn are indicators of degradation. For *ESR* and *C*, the estimation errors are less than 1%, and for $R_{ds,on}$ the estimation is less than 5%. Besides, this research seeks faults-diagnosis in PECs through measure-based techniques of voltage and current for capacitors, and MOSFET. In addition, fault detection and diagnosis methods for PEC must be able to operate in real conditions, i.e., with regulation control or even maximum power point tracking (MPPT) function in photovoltaic systems.

Acknowledgement

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Degradation indicators in power electronic converters

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Estimation of degradation indicators

To establish the degradation indicators of ESR, C, and $R_{ds,on}$, a Boost converter is used, as shown in Fig. 1,

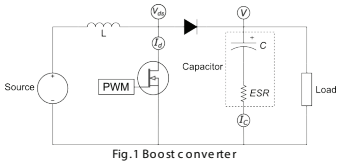

Fig.1 Boost converter

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Fig. 2. a) Technique of ohmic frequency range b)Technique for AC power losses

However, it is necessary the estimation of both parameters of the capacitor for establishing its degradation. For example, in previous work [2], a grid-connected photovoltaic system, both parameters, C, and ESR, of a DC-link capacitor were estimated using an electrochemical impedance spectroscopy (EIS) method. Estimation errors in Matlab/Simulink using three techniques present, are 0.087%, 0.026% only ESR. And the last technique for the parameters ESR and C are 0.53% and 0.37%, respectively.

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Illustration 1. Presented Poster at LAEDC 2022.

Sistema de monitoreo inteligente para motores completamente operativos

Intelligent monitoring system for fully operational engines

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Castillo-Picado, G.A; Fuentes-Quirós, G. Sistema de monitoreo inteligente para motores completamente operativos. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 29-34.

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Palabras clave

Prevención de daños; motores de inducción; voltaje; Arduino; ruido en motores; sensores; redes neuronales.

Resumen

La propuesta es realizar mediante el uso de Arduino y el uso de diferentes sensores, se pueda crear un sistema que pueda monitorear distintas condiciones de riesgo en motores trifásicos de inducción, como suministro de energía (corriente y voltaje), vibraciones y temperatura del motor o ambiente, para lo cual se utilizan sensores de vibración, de temperatura y sonoros, esto con intensión de verificar las condiciones del motor mediante el monitoreo. Esto puede evitar daños y perdidas en la producción con una detección temprana de estos factores, al notificar a los encargados en caso de estar en riesgo la integridad del motor y poder realizar en el sistema mantenimientos preventivos, los cuales tienen bajo costo y no retrasan tanto el proceso productivo como lo haría el realizar un mantenimiento correctivo, en el caso de daños en el motor o accesorios vinculados a este como es el caso de sistemas de ventilación, bombas y demás.

Keywords

Damage prevention; induction motors; voltage; Arduino; engine noise; sensors; neural networks.

Abstract

The proposal is made using Arduino and the use of different sensors, a system can be created that can monitor other risk conditions in three-phase induction motors, such as power supply (current and voltage), vibrations, and motor temperature or environment, for which vibration, temperature and sound sensors are used, this with the intensity of verifying the conditions of the motor through monitoring. This can prevent damage and production losses with early detection of these factors, by notifying managers if the integrity of the engine is at risk and being able to perform preventive maintenance on the system, which is low cost and does not take so long. the production process as would performing corrective maintenance, in the case of damage to the engine or related accessories such as ventilation systems, pumps, and others.

Introducción

A la hora de trabajar con motores de inducción en una industria, y se desea el bienestar de este durante largas jornadas en pleno funcionamiento, se expone a muchos posibles daños que pueden llegar a dañarlo y dejarlo fuera de operación durante un tiempo valioso, además de la dependencia de este para el proceso, un daño permanente en este, dependiendo del uso que se le dé, puede llegar a arruinar lotes completos de producción. Nuestro proyecto propone el monitoreo constante de motores mediante métodos no invasivos, utilizando microcontroladores y sensores, esto para poder observar el comportamiento tanto de picos de voltajes como corrientes altas y temperatura, que generan daños internos en el motor, con la variedad de estar siempre alerta a cualquier alteración ajena a las mencionadas anteriormente, estas alteraciones tanto en desfases mecánicos y demás pueden llegar a generar ciertos representaciones por sonido, esto es una señal de alerta de un funcionamiento no deseado del motor. Estas alteraciones se notificarán a la persona encargada en su móvil sobre la situación que está ocurriendo, para que ya con criterio técnico se apliquen planes de mantenimiento a los equipos o tomen la decisión que más beneficie a la empresa.

Materiales y métodos

Los motores de inducción trifásicas son muchas veces los ejes centrales de la producción de una empresa, cuando estos dejan de funcionar se detiene toda la maquinaria y lotes enteros de productos pueden llegarse a perder, el lograr predecir y mitigar esos fallos antes que sucedan, pueden mejorar la producción y disminuir el costo de reparación o sustitución del motor, a veces no aprovechamos las facilidades que nos puede traer un sistema de monitoreo, este combinado con método que nos alarme cuando existe un fallo para lograr erradicarlo antes que el motor deje de funcionar. Al ser estos motores afectados fácilmente por varias condiciones como una alimentación deficiente o en condiciones que el fabricante específicamente no recomienda, además de su situación ambiente donde estos motores al funcionar por medio de la inducción magnética, cualquier corto ocurrido por la situaciones presentes en el ambiente puede llegar a desenlaces fatales para todo el sistema relacionado al motor, ya sea que este mismo tenga como funcionalidad la movilización de bandas transportadoras, para tener ciertas zonas a cierta temperatura mediante la movilización de aire de forma externa o conectado a una bomba de agua en donde se necesita tener un flujo constante de agua para distintas utilidades, la importancia de que el motor se encuentre siempre en funcionamiento es vital en este tipo de situaciones. también se tiene que tomar en cuenta factores de temperatura en el ambiente del motor, esto debido a que cualquier proceso genera energía, muchas veces no toda la energía se aprovecha y es liberada, el agregar más calentamiento además del ya producido puede generar a largo plazo un daño en el motor.

Dentro de la problemática también estaría el hecho de no poder únicamente ser apagado el motor cuando se detecta alguna de las situaciones anteriormente dichas, debido a que cualquier alteración dependiendo el tipo de industria para el que se esté utilizando, puede llegar a generar perdidas, por lo que se necesita un sistema en el cual se pueda estar informado de la situación, de forma que preventivamente se puedan hacer los arreglos o mantenimientos preventivos para garantizar un buen estado del motor y con ellos el bienestar de la empresa

Resultados

Como el problema en cuestión lo sugiere, los motores de inducción presentan una gran diversidad de fallos, los picos de corriente, falla de fase, bajo voltaje y desbalance del voltaje, son de las principales razones, además de los daños que pueden generarse por un descuido del ambiente como lo es la vibraciones o temperatura, siempre que el motor presenta estos fallos se notara una alteración en los valores normales del motor, esto también expuesto por lo indicado por el fabricante de motor, como lo vemos en la siguiente figura:

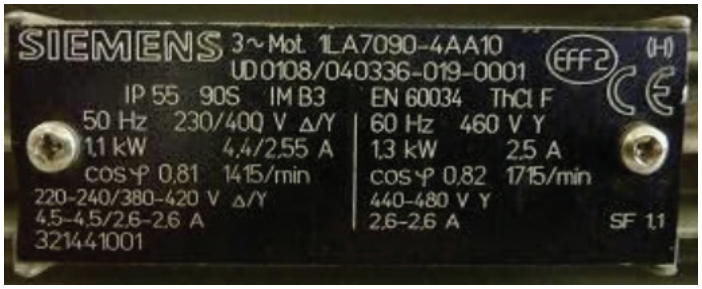

Figura 1. Datos de placa de motores sincrónicos.

En estas placas como se dijo anteriormente, el fabricante indica las condiciones para las cuales esta echa el motor, como lo es la temperatura, velocidad, conexiones, voltajes y corrientes entre otros datos. Con estos se puede establecer un estimado de condiciones de riesgo que no se

desean superar. En este caso, los motores indicados poseen una fuerza relativamente baja, siendo el más grande de 3 caballos de fuerza como se aprecia en la figura 1, la idea es que nuestra propuesta pueda ser de utilidad para motores de mayor que calibre que estos. Nuestra solución es introducir un sistema mediante múltiples sensores como lo vemos en la figura 2, que nos permita tener una respuesta más rápida y que nos pueda permitir actuar a tiempo para salvar el motor, constaría de varios sensores en tanto de temperatura, como sonoros y magnéticos, en donde generarían un sistema de monitoreo, estableciendo unas condiciones de normalidad en el sistema y también condiciones de alerta, en donde se notificara a los encargados para poder aplicar un arreglo preventivo, en donde por ejemplo se puede terminar un lote de producto que está en proceso para posteriormente realizar el mantenimiento del equipo o corrección del problema en cuestión, esto con la idea de no parar todo el proceso productivo de forma abrupta con riesgo de generar perdidas.

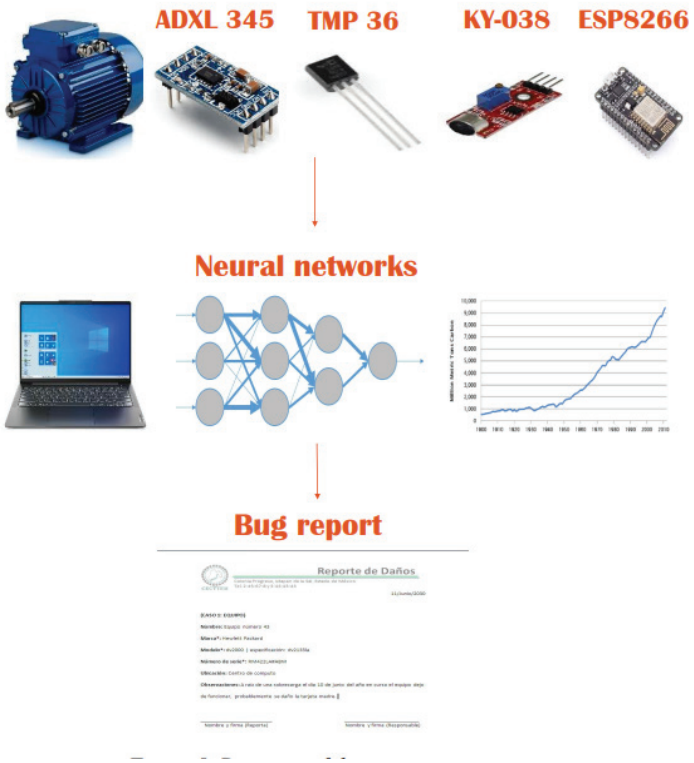

Figura 2. Diagrama del sistema de monitoreo.

1. Toma de datos por sensores: para este paso se van a disponer de tres sensores que nos permitan analizar el estado del sistema, se va a utilizar el sensor TMP 36, este se va a encargar de calcular la temperatura a la que está funcionando el sistema, un sensor de vibraciones ADXL 345 que permitan ver como se encuentra el entorno del motor, también se va a contar con un KY-003 que es el encargado de verificar la parte magnética del motor y por último el sensor de ruido KY-038, este será capaz de detectar las anomalías por medio del sonido.
2. Distribución de datos por Wifi: se va a utilizar el ESP8266 que es un chip que va a distribuir los datos del motor mediante wifi a una computadora que va a estar recibiendo todo lo que mande los sensores.

3. Programa de detección de fallas: se va a desarrollar un programa en base a la inteligencia artificial que analice los datos que distribuya el ESP 8266, donde se reciban la cantidad de una prueba por minuto, los datos van a ser estipulados por el usuario, conforme a lo que diga los datos de placa del motor, cuando el programa vea que estos datos son superados o no son acordes a la placa de datos, va a desarrollar un informe de la falla.
4. Reporte de averías del motor: cuando el programa detecte una anomalía en el funcionamiento del motor este va a emitir el informe fallas mediante una alerta en el teléfono y en la computadora del operario, la inteligencia artificial se va a ir alimentado en base a las anteriores fallas, esto en un tiempo va a tener la capacidad de dar un indicio de la falla, esto haciendo que no se dure tanto encontrando la falla y el paro de la producción no se alargue por mucho tiempo.
5. Ya el paso 5 es la solución del problema, después del monitoreo del problema, dado que se le notificó al operario a tiempo y pudo salvar el motor y el lote de producción.

Este sistema se va a tomar las bases de un mantenimiento preventivo, pero totalmente automatizado, donde se van a lograr dar el tratamiento adecuado a un motor brindando un tiempo de vida mas extendido, o por otro lado cuando se tiene una falla que es muy grande y sale muy costosa, poder estar prevenidos teniendo un repuesto antes de que falle, no afectando a la producción.

La implementación de este servicio en una empresa productora aseguraría tener los equipos en buenas condiciones, esto se ve reflejado en más cantidad de producción y que se va a poder producir con más calidad, haciendo que la empresa tenga más ganancias

Conclusiones y/o recomendaciones

El unir varias ramas de estudio puede generar una amplia gama de mejoras para una empresa, en nuestro proyecto decidimos unir la rama de dispositivos electrónicos, la rama de máquinas eléctricas y de inteligencia artificial, dando como resultado un sistema barato, eficiente y que tienen gran impacto en las empresas, aumentando ganancias y facilitando el trabajo.

Como ingenieros tenemos que procurar que los ejes principales de una empresa se mantenga en perfecto estado, el motor trifásico es utilizado por gran cantidad de empresas para diversas funcionalidades, por eso tenemos que asegurarnos que ese motor no nos vaya a fallar por un pico de voltaje o por no ingresar correctamente los datos de la placa, un sistema que monitoreo constante haría que se tenga certeza de que el equipo siempre va a estar en optimas condiciones o nos va a prevenir de un fallo, esto para que busquemos un remplazo y que no se tenga que parar la producción por mucho tiempo.

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LAEDC2022 LATIN AMERICAN ELECTRON DEVICES CONFERENCE

50 1971-2021 ANIVERSARIO TEC Tecnológico de Costa Rica

Intelligent monitoring system for fully operational engines.

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Introduction

When working with induction motors in an industry where the well-being of the motor is always desired during long hours in full operation, this exposes it to many possible damages.

Figure 1. Company with electric motors

Problem description

Three-phase induction motors are the central axes of a company's production, when they stop working, all the machinery stops, managing to mitigate these failures before they happen, can greatly reduce the costs of the company. Because these motors are easily affected by various conditions such as poor power, and temperature.

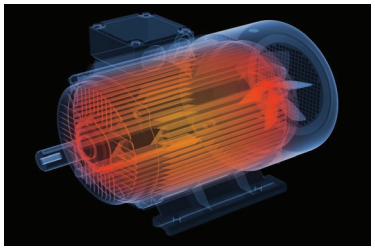

Figure 2. Overheating of a motor

peaks, phase failure, in addition to the damage that can be generated by the neglect of the environment such as vibrations or temperature. The motor presents these faults due to not taking into account the data on the motor plate.

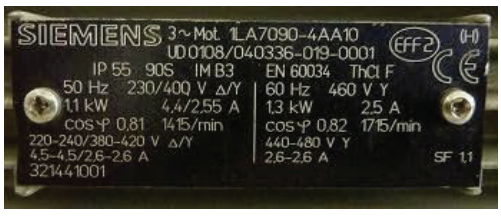

Figure 3: Nameplate data for synchronous motors

Currently, there are different monitoring equipment, only that these have high prices and still need a worker to review them, this presents a problem in response time.

Figure 4. Manual monitoring system

Problem solution

The solution is to introduce a system through multiple sensors. It would consist of several temperature, sound, and magnetic sensors. A monitoring system would be generated with the plate data that would be under the control of an artificial intelligence system.

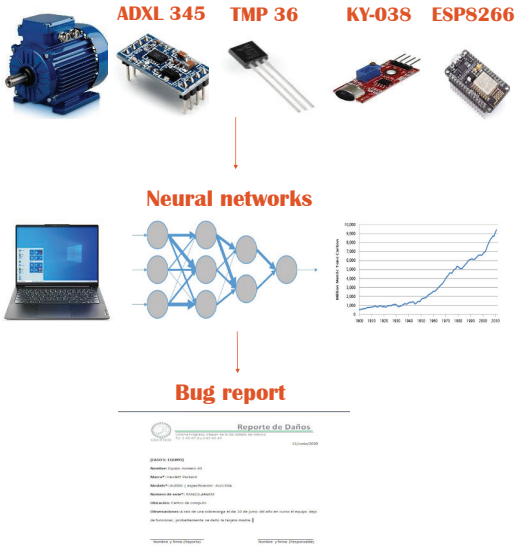

Figure 5. Diagram of the monitoring system

The TMP 36, ADXL 345, KY-003, and KY-038 sensors will be used, these will be able to detect anomalies, then ESP8266 will be used, which will distribute the engine data via Wi-Fi to a computer, it will develop an artificial intelligence program that analyzes the data and when there is a failure develops a report, which will be sent directly to the operator

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Ilustración 1. Póster presentado en LAEDC 2022.

Educación STEM a través del modelado e implementación de impresión 3D dentro de las áreas biomédica e industrial

STEM education through modeling and implementation of 3D printing within the biomedical and industrial areas

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Araya-Portuguez, K; Torres-Ulate, D. Educación STEM a través del modelado e implementación de impresión 3D dentro de las áreas biomédica e industrial. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 35-39.

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Palabras clave

Modelado 3D; impresión 3D; educación STEM; dispositivos electrónicos; biomedicina; estudiantes de secundaria; tecnología; innovación.

Resumen

El modelado e impresión 3D es una tecnología ampliamente utilizada. Puede ser utilizado en diferentes áreas de la industria como para imprimir dispositivos electrónicos como sensores y placas electrónicas, implementaciones dentro del área biomédica para fabricar prótesis y partes del cuerpo humano para preparación quirúrgica, o incluso dentro de industrias por ejemplo aeronáutica y automotriz. Todas estas aplicaciones y su importancia dentro de nuestra sociedad nos hacen requerir un mayor énfasis en las áreas de educación de tallos que involucran estas tecnologías. Por ello es que se considera que es de vital importancia enseñar esta relevante tecnología a personas jóvenes y creativas, que aún no están seguras de que camino tomar en su vida universitaria, un taller sobre estas tecnologías puede darle ese impulso que les falta para poder tomar una decisión y motivarse a innovar mediante la creación de diseños en modelado 3D por software y luego prototipar tanto en software como en impresión 3D.

Keywords

3D Modeling; 3D printing; STEM education; electron devices; biomedicine; high school students; technology; innovation.

Abstract

3D modeling and printing is a widely used technology. It can be used in different areas of the industry such as to print electronic devices such as sensors and electronic boards, implementations within the biomedical area to manufacture prostheses and parts of the human body for surgical preparation, or even within industries such as aeronautics and automotive. All of these applications and their importance within our society require us to place greater emphasis on the areas of stem education that involve these technologies. That is why it is considered vitally important to teach this relevant technology to young and creative people, who are still not sure which way to go in their university life, a workshop on these technologies can give them that boost they need to be able to take a decision and be motivated to innovate by creating designs in 3D modeling software and then prototyping in both software and 3D printing.

Introducción

En Costa Rica el conocimiento del modelado de piezas y La impresión 3D es baja, y muchas personas llegan a conocer las aplicaciones de esta importante rama de la ciencia y tecnología hasta llegar a una carrera universitaria, donde muchas veces solo se relaciona con un área de aplicación o pequeño enfoque relacionado con los procesos de fabricación [1]. Este problema suele estar relacionado con la poca enseñanza que está en esta área fuera de un currículo, lo que puede significar una falta de conocimiento del tema, esta falta de conocimiento puede significar una limitación a la hora de querer optimizar procesos o piezas innovadoras si por el contrario, tener conocimiento se genera una oportunidad para crear productos novedosos que pueden ser estudiados en detalle e incluso realizar simulaciones para buscar fallas, además de optimizar o resolver problemas, donde el principal la limitación es la creatividad y el ingenio. Actualmente, la impresión 3D se puede aplicar a la fabricación de algunos dispositivos

electrónicos [2], aunque esto es relativamente nuevo, es importante que las personas en están interesadas e investigan esto para que esto la tecnología tiene más investigación y experimentación que puede seguir creciendo, ya que imprimir estos dispositivos significa una gran ventaja para empresas o personas que trabajan con a ellos. Además, se puede aplicar la tecnología de impresión 3D a otras categorías, como la biomedicina, donde los innovadores han surgido ideas como la fabricación del cuerpo humano, piezas para preparaciones quirúrgicas, creación de prótesis, e incluso la creación de tejidos y órganos sintéticos que logran adaptarse al cuerpo, o en el caso de los industria aeroespacial y automotriz donde el uso de la tecnología mejora considerablemente algunas propiedades como como peso y resistencia.

Descripción del problema

Después de enfrentar una pandemia mundial y tener que cambiar drásticamente nuestros estilos de vida, es necesario proponer una metodología de enseñanza que combina los mejores aspectos de aprendizaje virtual y presencial [3] para enfatizar la enseñanza de los dispositivos electrónicos y la amplia gama de aplicaciones dentro del modelado 3D. Además, existe un problema que puede convertirse en el poca disponibilidad o dificultad de acceso a tecnología herramientas como equipo de cómputo dentro de las escuelas y universidades, pero como este problema es difícil de resolver, ideal es proponer estrategias que involucren a otros públicos instituciones como universidades para contribuir al STEM enseñanza de esta área de enfoque, a través de su tecnología equipos, dispositivos electrónicos y principalmente personas bien informado y entrenado en su operación, para combatir otro problema que es la importante falta de conocimiento sobre el uso del modelado y el uso de dispositivos electrónicos dentro de la impresión 3D que pueden representar un efecto dentro de la formación académica de los jóvenes, por ello, se propone enfatizar la enseñanza de temas como esta tecnología en la biomedicina [4] y sector industrial.

Propuesta de solución al problema

Entre los principales intereses de la educación STEM, se busca resolver el problema de la falta de conocimiento, que Es por ello que los jóvenes deben estar preparados en conceptos y herramientas que les dan la oportunidad de gestionar y comprender aspectos básicos en áreas de modelado y aplicaciones de la impresión 3D, esto a través de la explicación de conceptos y su respectiva ejemplificación para que los jóvenes pueden relacionar los diferentes dispositivos electrónicos presente en una impresora 3D y la función respectiva que cumplir, acompañado de las múltiples áreas de aplicación como las ya mencionadas dentro de la biomedicina y sector industrial, por lo que se propone dar unas pequeñas lecciones impartidas por alumnos y profesores de enseñanza superior educación que tienen conocimientos medios o avanzados en esta asignatura, estas lecciones se llevarían a cabo con el intención de generar interés en temas científico-tecnológicos y que con su realización se genera curiosidad y afán de investigación, además de el hecho de que de esta manera será posible dar una pequeña propuesta al estudiante sobre carreras universitarias que ser de interés o incluso actividades extraescolares que aumentar y reforzar sus conocimientos en la materia.

Siguientes pasos

Se realizará una lección que busca solucionar la falta de conocimiento en áreas STEM con énfasis en dispositivos electrónicos y su importancia en la impresión 3D, se buscará aplicar una metodología de enseñanza combinada con sesiones virtuales en las que se expondrán herramientas tecnológicas se utiliza para dar charlas introductorias que se graban y subido a

una plataforma de video para que los estudiantes puedan revisar los conceptos en cualquier momento que deseen y de forma presencial clases donde se aborda un enfoque computacional y se contará con laboratorios especializados en la materia facilitó para que pusieran en práctica todo aprendido y conocer los equipos de impresión 3D. Durante el desarrollo de las lecciones, se propone para mostrar lo que se puede hacer con el modelado y la impresión 3D en la fabricación de dispositivos electrónicos y biomedicina, este incluye la demostración de dispositivos de impresión tales como sensores o placas electrónicas, así como la impresión sintética Partes del cuerpo utilizadas para preparación quirúrgica, prótesis y equipo médico. Dado que es importante entender el funcionamiento de un impresora 3D, también habrá una pequeña visita guiada donde los participantes observan en detalle su estructura física y algunos dispositivos electrónicos que lo componen como finales de carrera mecánicos, sensores de temperatura, filamento sensores, finales de carrera ópticos, motores paso a paso, extrusores y placa base con su procesador, drivers y conectores además del importante papel que todos ellos jugar, trabajando juntos para realizar la impresión de piezas o dispositivos.

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LAEDC 2022 LATIN AMERICAN ELECTRON DEVICES CONFERENCE

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STEM education through modeling and implementation of 3D printing within the biomedical and industrial areas

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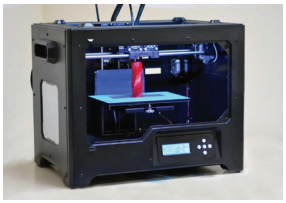
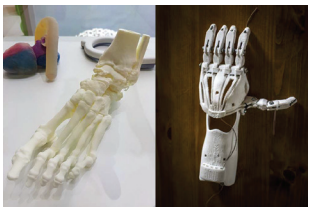
Introduction

3D modeling and printing is a technology that is widely used. It can be used to print electronic devices such as sensors and electronic boards in the biomedical area to manufacture prostheses and parts of the human body for surgical preparation.





Problem description

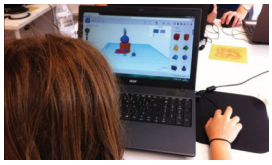
Currently, there is a lack of knowledge in engineering topics related to modeling and application of 3D modeling, due to the little equipment available in high school and the few experts in specialized application areas such as the creation of electronic devices and biomedical components with this technology.

Proposed solution

Propose a teaching methodology for high school students that combines the best aspects of virtual and face-to-face learning to emphasize the teaching of electronic devices and the wide range of applications within 3D modeling, such as biomedicine and the industrial areas.

Next Steps

A course will be held that seeks to solve the lack of knowledge in STEM areas with an emphasis on biomedicine, devices electronics and their importance in 3D printing, this seeks to apply a teaching methodology combined with virtual sessions which take advantage of technological tools.



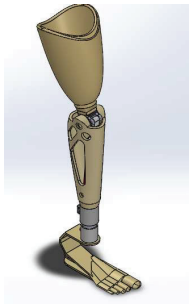


Ilustración 1. Póster presentado en LAEDC 2022.

Control Bucal para silla de ruedas

Mouth control for a wheelchair

Joel Sanabria-Salas[1]

Sanabria-Salas, J. Control bucal para silla de ruedas.
Tecnología en Marcha. Vol. 36, special issue. June, 2023.
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Palabras clave

Silla de ruedas; Arduino; control bucal; electronica; circuitos integrados.

Resumen

El proyecto propuesto consiste en ayudar y contribuir a la independencia y traslado para usuarios permanentes de sillas de ruedas que sufren de parálisis en sus extremidades y debido a esto no pueden operar ni controlar el movimiento de las sillas de ruedas eléctricas que existen hoy en día y deben ser asistidos por otra persona para el transporte, a través de un control bucal el cual funcionará como un dispositivo receptor de aire que conducirá el aire a sensores de presión conectados a un circuito Arduino o circuitos integrados lo que permite enviar la señal de movimiento a la silla y así dar una opción de independencia a las personas involucradas.

Keywords

Wheelchair; Arduino; mouth control; electronic; integrated circuits.

Abstract

The proposed project consists of helping and contributing to the independence of translation for permanent wheelchair users who suffer from paralysis in their extremities and due to this they cannot operate or control the movement of electric wheelchairs that exist today in the day and must be assisted by another person for transportation, through a mouth control which will function as an air receiving device that will lead the air to pressure sensors connected to an Arduino circuit or integrated circuits which allows sending the movement signal to the chair and thus give an option of independence to the people involved.

Introducción

Con la evolución del ser humano muchas áreas de la humanidad como la ciencia y tecnología también se han visto involucradas por lo que actualmente tenemos tecnología de punta para muchos de las áreas cotidianas en las que se desenvuelve el ser humano, por ejemplo podemos destacar la medicina, actualmente la mortalidad del ser humano se ha reducido todo gracias a los nuevos descubrimientos y avances medicinales, parte de ellos engloba las nuevas medidas para tratar enfermedades que años atrás se consideraban mortales, específicamente nos enfocaremos en los pacientes que han sufrido de amputaciones o que desde su nacimiento poseen algún problema de movilidad de sus extremidades y el único medio de movilidad que poseen es mediante una silla de ruedas impulsada por alguien, esta clase de situación provoca una dependencia de ambas partes, principalmente de la persona que se encuentra incapacitada de transportarse sola, con este proyecto se busca crear una alternativa de transporte o solución inmediata que pueda brindar una independencia a las personas

Materiales y métodos

Actualmente una cantidad entre 250 000 y 500 000 personas sufren de accidentes a nivel de su medula espinal lo cual provoca daños colaterales en las extremidades de la víctima, varios de estos efectos conllevan a una parálisis de extremidades englobándose en el término de tetraplejia que se refiere a la perdida de movilidad en las 4 extremidades (Brazos y piernas) otra de las afecciones la diplejía donde se pierde la movilidad del tren inferior y la parcialmente en el tren superior, al referirnos a un accidente podría ser sufrido por cualquier persona tanto joven

como adulto y si esta victima pierde su movilidad siendo una persona joven aún posee mucha vida por delante y será dependiendo de alguien por la indisposición de sus extremidades, dentro de este grupo de afectados se incluyen las personas que desde su nacimiento sufren de parálisis, muchos de estos casos son solamente afecciones a las extremidades y sus funciones neuronales son completamente normales por lo que se pueden desenvolver en el mundo de manera común en referencia a la interacción con el mundo a excepción de su movilidad y uso de extremidades, por lo que hasta el momento siempre se encuentran acompañados de personas que facilitan su transporte mediante una silla de ruedas, pero esto conlleva a la dependía de ambas, por parte del afectado necesita de alguien para su transporte y para la parte del transportador se requiere alguien con completa disposición que este siempre atento al cuido y transporte del afecto por estas situaciones, por lo que esta situación es un tanto injusta porque limita la independencia y vida propia de ambos.

La solución al problema en cuestión es facilitar un medio de independencia para las personas afectadas por tetraplejia y otros, para así pueden tener su propia libertad además de exentar las personas a su cargo, para esto lo que se desea proponer es un sistema controlado de manera oral el cual pueda ser adaptado a una silla de ruedas eléctrica o carrito eléctrico como los utilizados en los supermercados.

Figura 1. Silla de ruedas eléctrica.

En la imagen representada en la figura 1 se observa la silla eléctrica que existe actualmente y es vendida a usuarios para que cuenten con una autonomía propia de movimiento y transporte, si observamos su estructura determinamos que esta es controlada mediante un joystick el cual permite dar órdenes a la silla para producir el movimiento, sin embargo para usuarios con parálisis en su tren superior de extremidades se presenta una dificultad para el uso de estas ya que el joystick está diseñado para accionarlo con las manos, la propuesta es crear un dispositivo controlador para la silla el cual pueda ser accionado mediante la boca, ya que gran parte de la población solo presenta afección en sus extremidades mas no en las funciones realizables por su cabeza, el dispositivo se plantea mediante un circuito conformado por un controlador electrónico; ya se esté una placa Arduino o circuitos integrados donde se procesaran las ordenes de movimiento para la silla, la señal de activación será mediante sensores de presión la cual será activado mediante un soplido del usuario, se pretende crear un dispositivo bucal con al menos 5 canales para indicar las órdenes a la silla 4 direccionales básicas y un conducto de freno, se pretende que el usuario sople por el conducto de la dirección deseada y con tan solo un soplido leve el sensor capte el cambio de presión y envié la señal al controlador que haga mover la silla de manera constante en ese dirección hasta que el usuario sople el conducto de freno u otra dirección, esto para que no se necesite dar presión constante al sensor el usuario de mantener su soplido para el funcionamiento.

Resultados

Los pasos a seguir para el desarrollo de este proyecto consisten en la simulación digital del funcionamiento planteado ya que esto permite analizar el comportamiento de una manera económica sin riesgo de un prototipado fallido, una vez este funcione correctamente de manera digital se puede iniciar con la fabricación y conexión con la interfaz del joystick de una silla de ruedas eléctrica, una vez realizada la conexión se establece el ensamble del dispositivo de sensores que será interpretado por el Arduino.

Conclusiones

Esta propuesta facilitara el traslado para muchas personas que no poseen movilidad de sus extremidades permitiéndoles así una independencia de movimiento si la necesidad de otra persona que los ayude.

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Mouth electronic device control for wheelchair users

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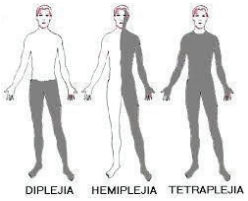
Introduction

We will focus on patients who have suffered from amputations or who since birth they have had some mobility problem in their limbs and the only means of mobility they have is through a wheelchair propelled by someone, this kind of situation causes a dependency on both parts, mainly on the person who is unable to transport himself alone, this project seeks to create an alternative transport or solution immediate that can provide independence to people.



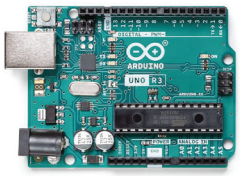
Problem Description

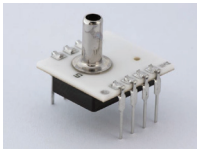
Currently, an amount between 250,000 and 500,000 people suffer from affections at the level of their spinal cord in an accident or since birth, this type of damage can trigger a paralysis of limbs in the victim, so up to now they are always accompanied by people who facilitate their transportation through a wheelchair, but this entails the dependency of both, on the part of the affected person needs someone to transport him and for the part of the transporter, someone with complete disposition is required who is always attentive to the care and transport of affection for these situation.

Solution Propose

We want to propose is a system controlled in a oral way which can be adapted to an electric wheelchair or electric cart such as those used in supermarkets.

if we observe its structure we determine that it is controlled by a joystick, however for users with paralysis in their upper limbs there is a difficulty in using them since the joystick is designed to be operated with the hands, the proposal is to create a controller device for the chair which can be operated through the mouth, because a large part of the population only has affection in their extremities but not in the functions that can be carried out by their head.
The device is proposed by means of a circuit made up of an electronic controller; Whether it is an Arduino board or integrated circuits where the movement orders for the chair will be processed, the activation signal will be through pressure sensors which will be activated by a user's breath





Next Steps

Create a prototype of circuit an buccal device to adapt them in a electric wheelchair instead of the directional joystick.

IEEE Advancing Technology for Humanity

2022 IEEE Latin American Electron Devices Conference (LAEDC)

Electron Devices Society

Ilustración 1. Póster presentado en LAEDC 2022.

Artificial Intelligence in STEM Education: Interactive Hands-on Environment using Open Source Electronic Platforms

Inteligencia Artificial en Educación STEM: Entorno Práctico Interactivo utilizando Plataformas Electrónicas de código abierto

Danny Xie-Li[1], Esteban Arias-Méndez[2]

Xie-Li, D; Arias-Méndez, E. Artificial intelligence in stem education: interactive hands-on environment using open source electronic platforms. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 45-52.

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Keywords

STEM Education; Artificial Intelligence; open source circuits.

Abstract

This article describes an interactive methodology to teach Artificial Intelligence (AI) through the contructivism philosophy of learning by doing, using, open source electronic platforms, like Arduino, Snap Circuits, Raspberry Pi and Circuit Playground, with an interactive hands-on approach Workshops. These are provided to high school and non-engineering students by (previously trained) engineering students volunteers. The methodology proposed is designed to highlight, in different learning activities, key concepts about Artificial Intelligence (AI). AI abstractes the human intelligence processes through algorithms and computer systems, taking advantage of the amount of data generated nowadays to create innovative, effective, efficient, accurate and at low cost solutions, applied in different fields. The main purpose is to motivate the participants to explode its creativity, improving their innovation skills to provide solutions for XXI century problems, better quality of life, health, among others. A survey will be conducted for the students to find insights about effectiveness of the proposed methodology to better acquire knowledge about AI knowledge. We encourage instructors to use similar interactive hands-on methodologies and to include AI concepts with STEM activities into general education courses. Other concerns of AI, is about the fairness of these algorithms, the inclusion and diversity is a key player in how these systems are built, and it can have consequences as the person perspective when building it The idea of the need for diversity and inclusion of the AI field.

Palabras clave

Educación STEM; Inteligencia Artificial; Circuitos de código abierto.

Resumen

Este artículo describe una metodología interactiva para enseñar Inteligencia Artificial (IA) a través de la filosofía del contructivismo de aprender haciendo, utilizando, plataformas electrónicas de código abierto, como Arduino, Snap Circuits, Raspberry Pi y Circuit Playground, con un enfoque práctico interactivo Talleres. Estos se imparten a estudiantes de secundaria y no ingenieros por voluntarios (previamente formados) estudiantes de ingeniería. La metodología propuesta está diseñada para destacar, en diferentes actividades de aprendizaje, conceptos clave sobre la Inteligencia Artificial (IA). La IA abstrae los procesos de la inteligencia humana a través de algoritmos y sistemas informáticos, aprovechando la cantidad de datos que se generan hoy en día para crear soluciones innovadoras, eficaces, eficientes, precisas y a bajo coste, aplicadas en diferentes campos. El propósito principal es motivar a los participantes a explotar su creatividad, mejorando sus habilidades de innovación para dar soluciones a problemas del siglo XXI, mejor calidad de vida, salud, entre otros. Se realizará una encuesta a los alumnos para conocer la efectividad de la metodología propuesta para adquirir mejor los conocimientos sobre IA. Animamos a los instructores a utilizar metodologías interactivas similares y a incluir conceptos de IA con actividades STEM en los cursos de educación general. Otra de las preocupaciones de la IA, es sobre la equidad de estos algoritmos, la inclusión y la diversidad es un jugador clave en la forma en que estos sistemas se construyen, y puede tener consecuencias como la perspectiva de la persona al construir La idea de la necesidad de la diversidad y la inclusión del campo de la IA.

Introducción

Artificial intelligence (AI) is an interdisciplinary broadly technology in the area of computer science that abstract human cognitive behaviors to create intelligent systems, the emerging of AI has been used, surrounded in applications to solve complex problems and becoming an important disruptive force that provides significant impact in the society [9]; applications can be included in different areas from healthcare, agriculture, automotive, robotics to especially education. In addition, another common field that started to emerge is the robotic field, in which we can find robots in our daily lives, it is important to include them in the education process as well. Besides the inclusion of AI in education, researchers have explored the possibility of teaching AI knowledge into the general learning curriculum to prepare the future for students in STEAM (Science, Technology, Engineering, Arts and Mathematics) fields [1]. But not all the students in Costa Rica have access to robotics.

STEAM Education and AI

AI literacy, recognized as a set of skills, includes technological attitudes, abilities and competencies that people use AI effectively and ethically to solve problems in daily life [10]. To introduce AI knowledge we proposed the use of open source platforms that includes Arduino, Snap Circuits, Raspberry requires creativity and innovative approaches to abstract complex concepts into simple understandable knowledge based on interactive hands-on activities with modular electronic components based on the constructivist philosophy. The authors explored the possibility to teach AI knowledge to high school and non-engineering students exposing the students in STEAM fields, to develop and power the AI literacy set skills, highlighting the awareness of potential ethical issues in the field of AI.

Inclusion and gender diversity

We still find gender imbalance and exclusion in different ways in our society of any form of discrimination, based on gender stereotypes, unfair distribution of power, exclusion based on groups, such as race, class, language, ethnicity, gender, sexual orientation. Leading to a negative environment for minority groups representation, which should be an important concern to address in STEAM education [12]. The authors [12] exposed educational robotics is one resource to promote inclusion, interaction, interdisciplinarity, problem solving, and collaborative work, developing a set skills and cross-functional learning, including: teamwork, cooperative learning, leadership, entrepreneurship, logical thinking, psychomotricity, creativity, curiosity, concentration, and mathematics.

In this article, we present a project initiative to offer a course that consists of a set of workshops on educational artificial intelligence based on the constructivist and constructionism philosophy using open source circuits, like Arduino, Circuit Playground, Raspberry, Snap Circuit, driven by university students engineering volunteers to promote diversity and inclusion in STEAM fields for high school and non-engineering students.

Literature Review

Learning by doing in hands-on activities, based on constructivist and constructionism philosophy usually generalized as the concept related to the result of the learner experience and interaction with the world, allowing the person to learn on his/her own, encouraging the students

to deepen the knowledge avoiding memorization, acquiring meaningful context to understand the concepts. Different previous works have proposed hands-on activities indicated in [2], [3], [4], [5], [6], [7], [8] that achieved student engagement in STEAM fields.

A case of study of a program of ten lessons divided into four modules, proposed by the authors [13], examines the robotics applicability to teaching STEAM subjects in public High Schools, the results of the perception of the students about the course reported that 61.2% tend to STEAM subjects, and 22.7% neutral and 9% low affinity, in addition, the influence of female in STEAM-fields is related to social influence and construct given more importance in early stages.

Authors in [14] explored the educational robotics, a learning tool utilized in science units for 4th grade students for enhancing learning in STEM knowledge and skills, hightled students engaging in the work of building and programming autonomous robots, and concluded the effectiveness of the learning standards required by many states.

Methodology

Educational Artificial Intelligence with Open Source Electronic Platforms

Participants

The course has no cost associated, designed to target high school and non-engineering participants to offer equal, in groups of 20-30 students ranging in age between 15-20 years old to participate in this set of workshops. Students are going to be registered and selected preferably from local and rural public institutions, the objective is to reach as many participants as possible offering equal possibilities for all parties.

Tutors

Tutors teams integrated based on volunteer students from local universities in engineering domains in collaboration with IEEE support [6], the tutors design their own material using the creativity, innovation to be comfortable for them based on the course defined to teach.

Main goals

- Enforce the self-confidence of underrepresented students and disciplines.
- Enrich STEAM concepts in the classes curriculum.
- Incite critical thinking, problem solving, teamwork, leadership, debug abilities, and allow the students to feel comfortable in making mistakes.
- Motivate the idea of the need for diversity, inclusion, and representation of different fields of science in AI research and industry.
- Encourage and incorporate AI in an ethical manner that benefits society.

Program design

Module	Submodule	Content	Fields
Basics in Circuit Playground and Artificial Intelligence	Basics in Circuit Playground	Arduino idle software, Circuit Playground board,	Software and Hardware definitions.
	Introduction to Algorithms and Artificial Intelligence	Initial concepts in programming and artificial intelligence.	Software and Artificial Intelligence definitions.
Building the first led neuron.	Inputs and outputs from the environment	Inputs and Outputs of the Circuit Playground used to capture information from the environment	Software and Hardware
	Getting started with patterns	Initial concepts in pattern recognition	Software
	Introduction of perceptron algorithm	Perceptron, two-class (binary) classification algorithm	Software
Fruit color detection	Light sensor	Photodetector as an input information	Hardware and Software
Piano color fruit	Speaker module	Using the speaker module as an output of the sound wave	Hardware and Software

Basics in Arduino and Artificial Intelligence

The introductory module, students will first be presented with the introductory concepts of logical programming, artificial intelligence basic concepts and Circuit Playground board, such as Circuit Playground board components and idle software. The students will conduct assignments in practice to turn on the leds of the Circuit Playground Board. In the second submodule, students will learn more advanced subjects, such as algorithms, using the Arduino idle software, at this point students will learn basic concepts of artificial intelligence and the bioinspiration of computer and biology related to artificial intelligence.

Building the first led neuron

In this module, the students will be introduced to the subject of pattern recognition to solve problems involving Circuit Playground, utilizing new and more advanced functions to build a basic neuron, the perceptron algorithm, using the sensors included in the board as an input and the leds as outputs, with the goal to identify the pattern and understand how to capture information from the environment and return an output to the environment. At the end of the lesson the students who completed the essential tasks will be assigned in equally assigned groups to solve other pattern recognition tasks involving the circuit playground board.

Fruit color detection

In these modules sessions focus on the second part of the pattern recognition subject. Given a Circuit playground board with different fruits with his own distinct color characteristic, using the light sensors included in the board and the led's, to identify the fruit based on the color, the method of this session is to make teamwork using the divide-conquer approach in a limited time to solve the problem. This is an incentive to build teamwork, communication, manage time and debugging skills.

Piano color fruit

At this point, students will start to work to solve more complex problems, involving the subject of pattern recognition putting everything together of the learned modules, using inputs and outputs from the environment, and the perceptron as a learning algorithm, to identify fruit colors to convert the information into sound waves of piano sheet music. Will be given the circuit playground board and speaker modules. The method for this session is to build and share, given a limited amount of time for one student, the next student needs to continue the work of the previous student until completed or solved the problem. This incite creativity, allow introspective students to feel comfortable, teamwork, communication, sharing and inclusiveness.

Tools

For these sessions the Circuit Playground by Adafruit will be used as a board and the Arduino IDE software to program the code, and load into the board. The Circuit Playground board is a ATmega32u4 micro-processor running at 3.3V and 8MHz, that can be powered from USB or AAA battery. The board comes with 10 mini NeoPixels, 1 motion sensor, 1 temperature sensor, 1 light sensor, 1 sound sensor, 1 mini speaker, 2 push buttons, 1 slide switch, 8 alligator-clip friendly input/output pins, that can act as capacitive touch inputs, red led and reset button [15]. The sensors help to capture information such as motion, light, sound, temperature from the environment. The speaker, leds, and NeoPixels can act as output signals to the environment to provide a feedback loop. The board is programmed using the Arduino IDLE, it uses a wiring language framework of a simplified version of C/C++ programming language. This allows the students to get familiar with the programming language and motivates them to get curious and understand some programming principles.

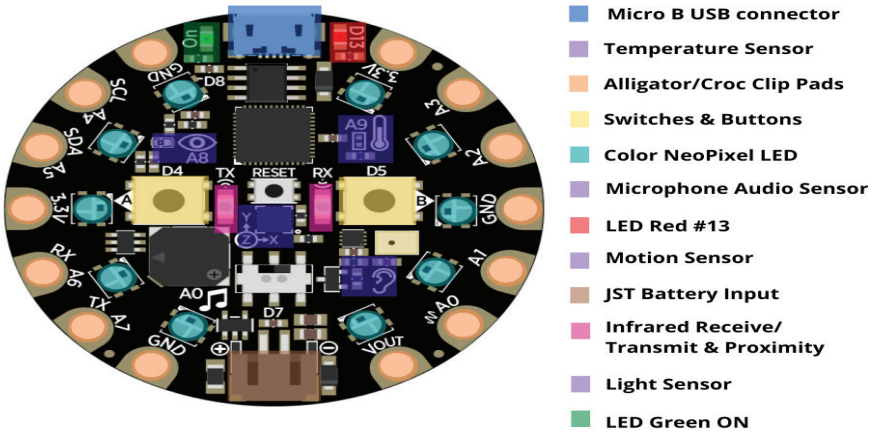

Figure 1. Circuit Playground Express board from Adafruit and the components.
(Image taken from: https://github.com/adafruit/Fritzing-Library)

Course structure

The course is composed of 4 modules design to be a two week plan, started from initial and introductory concepts and getting familiar with the tools, following applying the knowledge in hands-on tasks-projects with progression in complexity

Evaluation of the methodology

To evaluate the achievement of the goals of the project a qualitative and quantitative assessment approach is proposed to conduct the evaluation with the students, to protect the data privacy, this will be carried out anonymously. For the qualitative approach, the students need to log

their experiences in an audio-recorded with explanations and reflections about their learning. In addition, the tutors' will log the observations during the course activities to study student feelings. For the quantitative assessment, questionnaires and interviews were proposed using online forms as Google Forms to evaluate students' prior knowledge, learning experiences and conceptual knowledge acquired from the workshops.

Next steps/ Future work

The next steps involve recluting volunteer engineering students from local universities and preparing pedagogical material, to execute the methodology in local rural high schools and non-engineering students, in a period of 6 weeks, with the financial support of IEEE [6], and evaluate the effectiveness of the methodology through quantitative and qualitative evaluations to measure accomplish of the goals defined.

A future work should aim to extend the methodology to teach AI STEAM education with Arduino, Raspberry Pi, Snap Circuits and other open source boards to identify the advantages and disadvantages to use different boards to introduce AI in STEAM education through open source boards.

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Artificial Intelligence in STEAM Education: Interactive Hands-on Environment using Open Source Electronic Platforms

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Abstract. This article describes an interactive methodology to teach **Artificial Intelligence** (AI) through the **contructivism philosophy** of learning by doing, using, **open source electronic platforms**, like Arduino, Snap Circuits, Raspberry Pi and Circuit Playground, with an interactive hands-on approach **Workshops**. The methodology proposed is designed to highlight, in different learning activities, key concepts about Artificial Intelligence (AI). The main purpose is to motivate the participants to explode its **creativity**, improving their **innovation** skills to provide **solutions** for XXI century problems, better quality of life, health, environment, entertainment, among others. Other concerns of AI, is about the **fairness** of these algorithms, the **inclusion** and **diversity** is a key player in how these systems are built, and it can have consequences as the person perspective when building it The idea of the need for diversity and inclusion of the **AI field**.

Keywords. STEAM Education, Artificial Intelligence, Open Source, Circuits.

I Introduction

Artificial intelligence (AI) is an interdisciplinary broadly technology in the area of computer science that abstract **human cognitive** behaviors to create **intelligent systems**, the emerging of AI has been used, surrounded in applications to solve complex problems and becoming an important **disruptive force** that provides significant impact in the **society**. Researchers have explored the possibility of teaching **AI knowledge** into the general learning curriculum to prepare the future for students in **STEM fields**. [1]

- STEM Education and AI
- Inclusion and gender diversity

Figure 1. Iterative methodology for AI+STEM Education workshops improvements.

III Future Work

The next steps involve:

- Recluting **volunteer engineering** students from local universities and preparing **pedagogical material** supported by IEEE [2], to execute the methodology in **local rural high schools** and **non-engineering** students,
- Evaluate the effectiveness of the methodology through **quantitative** and **qualitative** evaluations to measure accomplish of the **goals** defined.
- In addition extend the methodology to teach **AI STEM education** with **Arduino**, **Raspberry Pi**, **Snap Circuits** and other open source boards to identify the effectiveness to use different boards to introduce AI in STEM education through **open source boards**.

Figure 2. AI+STEM Education.

II Methodology

Participants. High school and non-engineering participants to **offer equal**, in age between 15-20 years old offering **equal possibilities** for all parties. ***Tutors.*** Design their own material, integrated based on **volunteer students** from local universities in engineering domains. ***Tools.*** **Circuit Playground** by Adafruit will be used as a board and the **Arduino IDE** software to program the code, and load into the board.

Main goals.

- Enforce the **self-confidence** of **underrepresented students** and disciplines.
- Incite **critical thinking**, **problem solving**, **teamwork**, **leadership**, **debugging** skills and allow the students to **feel comfortable** in making mistakes.
- Motivate the idea of the need for **diversity**, **inclusion**, and representation of different fields of science in **AI research** and **industry**.
- Encourage and incorporate AI in an **ethical** manner that benefits society.

Evaluation of the methodology.

Qualitative and **quantitative** assessment approach is proposed to conduct the evaluation with the students.

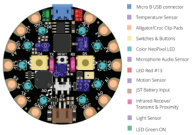

Figure 3. Components of the Circuit Playground Express Board by AdaFruit. (Image taken from: https://github.com/adafruit/Fritzing-Library)

Module	Submodule	Content	Fields
Basics in Circuit Playground and Artificial Intelligence	Basics in Circuit Playground	Arduino idle software, Circuit Playground board,	Software and Hardware definitions.
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	Introduction of perceptron algorithm	Perceptron, two-class (binary) classification algorithm	Software
Fruit color detection	Light sensor	Photodetector as an input information	Hardware and Software
Piano color fruit	Speaker module	Using the speaker module as an output of the sound wave	Hardware and Software

Table 1. Program design. Workshops for AI+STEM Education

Reference
[1] B. Sakulkueakulsuk et al., "Kids making AI: Integrating Machine Learning, Gamification, and Social Context in STEM Education," 2018 IEEE International Conference on Teaching, Assessment, and Learning for Engineering (TALE), 2018, pp. 1005-1010, doi: 10.1109/TALE.2018.8615249.
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IEEE Electron Devices Society

Ilustración 1. Póster presentado en LAEDC 2022.

Feasibility study for the implementation of number portability in Nicaragua

Estudio de factibilidad para la implementación de la portabilidad numérica en Nicaragua

Guillermo de Jesús Valdivia-Medina[1]

Valdivia-Medina, G.J. Feasibility study for the implementation of number portability in Nicaragua. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 53-58.

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Keywords

Number Portability; Centralized Database; Administrator; All-Call Query; TELCOR; Regulation.

Abstract

The document “Feasibility Study for the Implementation of Number Portability in Nicaragua” proposes the mechanisms to implement operator Number Portability, taking into account the ITU-T Series Q and E regulations. The existing information is analyzed, after the collection of information through interviews with operator officials, as well as surveys of users of telephone services. After reviewing the advantages and conditions of the different techniques to implement number portability, we recommend the All Call Query technique, a simple and effective method, as well as operator Number Portability, for which you need intelligent network capabilities to recognize the ported number, the status, the conditions and the operator must develop activities to adapt their networks to this model. The documents that legally and regulatory support the implementation of Number Portability are: Administrative Agreement No. 036-2003, the Numbering Resource Regulations and the National Numbering Plan, all of these issued by TELCOR Regulatory Entity, the Free Trade Agreement between the Dominican Republic - Central America and the United States (DR-CAFTA) and the Regional Technical Telecommunications Commission of Central America, COMTELCA The elaboration of regulatory documents such as the Number Portability Regulation is proposed and indications are given for the creation of the Centralized Database Administrator with its subordinates in the different nodes that make up the network and a proposal for a General Implementation Plan.

Palabras clave

Portabilidad numérica; Base de datos centralizada; Administrador; Consulta general; TELCOR; Regulación.

Resumen

El documento “Estudio de Viabilidad para la Implementación de la Portabilidad Numérica en Nicaragua” propone los mecanismos para implementar la Portabilidad Numérica de operador, tomando en cuenta la normativa UIT-T Serie Q y E. Se analiza la información existente, luego de la recolección de información mediante las entrevistas a funcionarios de las operadoras, así como encuestas a usuarios de los servicios telefónicos. Después de revisar las ventajas y condiciones de las diferentes técnicas para implementar la portabilidad numérica, recomendamos la técnica de Consulta de Todas las Llamadas (All Call Query), método sencillo y eficaz, así como la Portabilidad Numérica de operador, para lo cual se necesita capacidades de red inteligente para reconocer el número portado, el estado, las condiciones y el operador debe desarrollar actividades para adecuar sus redes a este modelo. Los documentos que avalan de forma jurídica y regulatoria la implementación de la Portabilidad Numérica son: el Acuerdo Administrativo nº 036-2003, el Reglamento del Recurso de Numeración y Plan Nacional de Numeración, todos estos emitidos por TELCOR Ente Regulador, el Tratado de Libre Comercio entre la República Dominicana - Centroamérica y los Estados Unidos (DR-CAFTA) y la Comisión Técnica Regional de Telecomunicaciones de Centroamérica, COMTELCA. Se propone la elaboración de documentos de regulación como el Reglamento de Portabilidad Numérica y se dan indicaciones para la creación del Administrador de la Base de Datos Centralizada con sus secundarios en los diferentes nodos que conforman la red y una propuesta de un Plan General de Implementación.

Introduction

After the privatization of telecommunications in Nicaragua, the first telephone company “Nicacel” emerged. The first telecommunications laws were established and regulatory bodies such as the Nicaraguan Institute of Telecommunications and Post Office (TELCOR) were created.

TELCOR issues the enabling titles for operators such as: concession contracts, permits, licenses, among others. The authorized cell phone operators are Claro, Tigo and Cootel. Each one has its particularities that the user analyzes to subscribe to the company, many times they do not meet expectations and they take it for the need to communicate. The drawbacks are: the price, the coverage and the quality of the service, this determines the client’s satisfaction with the service acquired.

Data collection is carried out through interviews with operator officials and surveys of users of telephone services.

The structure of the numbering system is analyzed, as well as the routing of calls and its security, in addition, a comparison is made between several countries with similar characteristics to Nicaragua. An analysis of the legal basis in the field of telecommunications is carried out to justify its implementation and the need for it, as well as the benefits it brings to users, operators and commerce in general.

The purpose of implementing Number Portability in this study is to carry out a technical and legal analysis so that users conceive Number Portability as a right to maintain their telephone numbers regardless of the operator, service or geographical position of the users, when they for reasons quality of service, costs, location, etc. decide to change provider, service or geographic area. In this sense, it becomes an important agent for the development of competition between service operators.

Objetives

Overall Objective

- Propose the procedure for the feasibility of Number Portability through the standards and legal bases of the ITU-T Series Q, E, in order to make a comparison between countries and know the degree of knowledge of the main actors involved.

Specific Objectives

- Collect and analyze information on Number Portability through user surveys and interviews with operator officials to measure the degree of knowledge of the different main actors involved in Nicaragua.
- Carry out a comparison between countries to determine applicable methods in Nicaragua.
- Use the standards of the ITU-T Series Q, E.

Implementation description

All-Call Query

This model consists of the generation of a Centralized Database, which contains information on telephone numbers, which will be used by mobile operators to route a call.

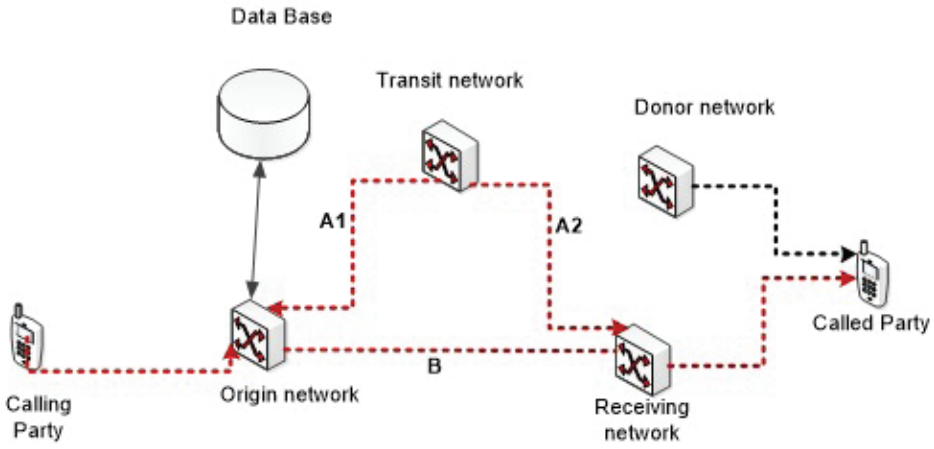

Figure 1. Routing initiated according to the principles of the query to every call.

The illustration shows that the Originating Network (RO) has access to the database (DB) of ported numbers (PN) with the full address of the receiving center. This indicates that only one database query is needed to complete the call, it is possible that more than one database query is needed, the donor network (RD) is not involved in establishing the call [1].

Database Administrator

To manage the portability of numbers, a centralized database (DB) is implemented that contains the ported numbers and to which the operators connect to keep their own database updated and thus establish communication with the ported number

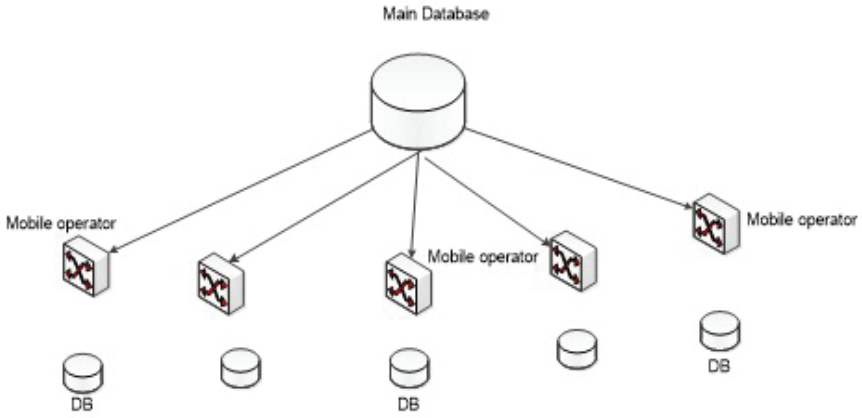

Figure 2. Database administrator.

Investigative development

Country	Law of PN	PN Regulation	PN implemented	Implementation date	Routing scheme	Number of ported numbers	Database administration	Time to port the number	Cost
Nicaragua	No	No	Not applicable	Undetermined	undetermined	Not applicable	Not applicable	Not applicable	Not applicable
Costa Rica	No	Yes	yes	30/11/2013	All-Call Quey	1,9 M	Cortes Ingles	48 Hours	None
Honduras	yes	Yes	yes	30/4/2014	All-Call Quey	206,338	Systor International	5 Minutes	None
Republica Dominica	no	Yes	yes	30/9/2009	All-Call Quey	8000	Cortes Ingles	24 Hours	None
Peru	yes	Yes	yes	1/10/2010	All-Call Quey	1,1 M	Cortes Ingles	24 Hours	None
El Salvador	yes	Yes	yes	24/8/2015	All-Call Quey	3,6	Imcard Mediafon	1-3 hours	None

Figure 3. Comparative table of the countries of the Free Trade Agreement DR-CAFTA and Peru on the implementation of Number Portability.

Unlike Nicaragua, all these countries have already implemented number portability and there is experience in this service aimed at the population as a right. All have implemented the ITU-T Q-series Supplement 2 All Call Query method. They all have a Database Administrator, highlighting the Spanish autonomous entity EL CORTE INGLES [2].

Supplement 2 to Recommendation ITU-T E.164 defines a standardized terminology for Number Portability within an ITU-T E.164 numbering system. Numbering and addressing formats, call flows, network architectures, and routing approaches are defined. [3].

Q-series Supplement 3 describes number portability from the standpoint of high-level service definitions and terminology and presents a set of high-level network architectures and generic routing methods for number portability. [4].

Conclusion

The procedure for the feasibility of number portability with the ITU-T Series Q, E standards is proposed, with the routing described in the All Call Query method.

The study and analysis of the information obtained from TELCOR, CANITEL, the UIT-T and COMTELCA, from the experiences and knowledge of mobile users and other operators that have implemented Number Portability, was very useful for the feasibility proposal of number portability. Implementation is possible with fewer resources and less time than in other countries.

The operators must have the right environment and the minimum impact on the implementation. TELCOR should be in charge of carrying out the number portability, this may result in an additional cost to the annual budget already established by the operator.

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Feasibility Study for the Implementation of Number Portability in Nicaragua

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Introduction

In Nicaragua, the number portability service does not exist, since the initiative has not been taken and the operators are reluctant to implement it. TELCOR, regulatory entity, issues enabling titles such as: concession contracts, permits, licenses, among others.

The authorized mobile operators are Claro, Tigo and Cootel. Each one has its particularities that the user analyzes to subscribe to an operator, many times they do not meet expectations and they take it for the need to communicate. The drawbacks are: price, coverage and quality of service. Data collection is carried out through interviews with operator officials and surveys of telephone service users.

The structure of the numbering system is analyzed, as well as the routing of calls and their security, in addition, a comparison is made between several countries with similar characteristics to Nicaragua. An analysis is carried out to justify its implementation, as well as the benefits it brings to users, operators and commerce in general. The purpose of implementing Number Portability is to carry out a technical and legal analysis so that users conceive Number Portability as a right to maintain their telephone numbers regardless of the operator, service or geographical position of the users, when for reasons of quality of service, costs, location, etc. decide to change your provider, service, or geographic area

Investigative Development

Country	Law of PN	PN Regulation	PN Implemented	Implementation date	Routing scheme	Number of ported numbers	Database administration	Time to port the number	Cost
Nicaragua	No	No	Not applicable	Undetermined	undetermined	Not applicable	Not applicable	Not applicable	Not applicable
Costa Rica	No	Yes	yes	30/11/2013	All-Call Query	1.9 M	Cortes ingles	48 Hours	None
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Peru	yes	Yes	yes	1/10/2010	All-Call Query	1.1 M	Cortes ingles	24 Hours	None
El Salvador	yes	Yes	yes	24/8/2015	All-Call Query	3,6	Imcard Mediafon	1-3 hours	None

Unlike Nicaragua, all these countries have already implemented number portability for years, there is already experience in managing this type of service, which is addressed to the population as a right.

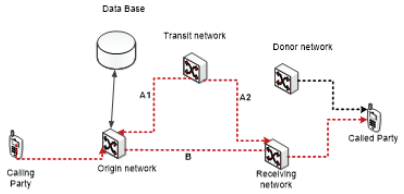
They have all implemented the routing scheme described in the ITU-T Q-series Supplement 2 All Call Query method.
They all have a Database Administrator, with the Spanish independent entity EL CORTE INGLES standing out.

Supplement 2 to Recommendation ITU-T E.164 defines a standardized terminology for Number Portability within an ITU-T E.164 numbering system. Numbering and addressing formats, call flows, network architectures, and routing approaches are defined.

Q-series Supplement 3 describes number portability from the standpoint of high-level service definitions and terminology and presents a set of high-level network architectures and generic routing methods for number portability.

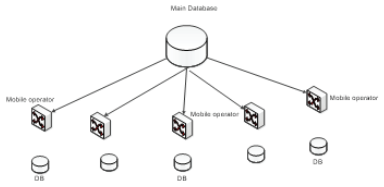
Implementation Description

The All-Call Query model consists of the generation of a Centralized Database, which contains information on telephone numbers, which will be used by mobile operators to route a call.



Routing initiated according to the principles of the query to every call.

To manage the porting of numbers through the ACQ modality, it is necessary to implement a centralized database (DB) which contains the universe of ported numbers in operation and to which the Network and Service Providers must connect to keep their own database updated. BD of operation in order that, at the time of the communication, it is connected to the network where the destination user number is located and communication is established.



Conclusions

The procedure for the feasibility of number portability with the ITU-T Series Q, E standards is proposed, with the routing described in the All Call Query method.

The study and analysis of the information obtained from TELCOR, CANITEL, the UIT-T and COMTELCA, from the experiences and knowledge of mobile users and other operators that have implemented Number Portability, was very useful for the feasibility proposal of number portability. Implementation is possible with fewer resources and less time than in other countries.

Regarding the acceptance by the operators, the recommendations are to give them the right environment so that the impact on their structure is minimal and the transition does not present a major inconvenience. However, TELCOR will have to take care of the financing between the operators and the entity in charge of portability, which represents an additional cost to the annual budget already established by the operator.

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Electron Devices Society

Illustration 1. Presented Poster at LAEDC 2022.

Analysis of the stability of organic photovoltaic cells under indoor illumination

Análisis de la estabilidad de celdas fotovoltaicas orgánicas bajo iluminación interior

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Keywords

Degradation Analysis; encapsulated solar cells; current density-voltage; organic solar cells; PTB7:PC70BM; indoor illumination.

Abstract

In this study, we analyze the degradation behavior of conventional polymeric solar cells (PSCs) under constant indoor light illumination. A LED lamp with a color temperature of 2700 K, was used for the indoor light illumination conditions. We compare the results obtained with encapsulated and non-encapsulated devices. The performance of the PTB7:PC_{70}BM-based cell showed an initial maximum power conversion efficiency (PCE) of 12.0% under the luminance of 1000 lux and maximum power density (MPP) of 45.7 μW/cm^2. The work describes the results of the measurements and analysis of the degradation process, performed by a current density – voltage (J–V) characteristic curve study under LED light. The analyzed performance parameters were PCE, short circuit current density (J_{SC}), open-circuit voltage (V_{OC}) and fill factor (FF). The PCE of encapsulated devices remained above 80% of the initial value after 624 h.

Palabras clave

Análisis de degradación; celdas solares encapsuladas; densidad de corriente-voltaje; celdas solares orgánicas; PTB7:PC70BM; iluminación interior.

Resumen

En este estudio, nosotros analizamos el comportamiento de degradación de celdas solares poliméricas convencionales (PSCs) bajo iluminación de luz interior constante. Para las condiciones de iluminación de luz interior se utilizó una lampara LED con una temperatura de color de 2700 K. Nosotros comparamos los resultados obtenidos con dispositivos encapsulados y no encapsulados. El desempeño de las celdas basadas en PTB7:PC_{70}BM muestra una eficiencia de conversión de potencia máxima (PCE) inicial de 12.0% bajo la iluminancia de 100 lux y una densidad de potencia máxima de 45.7 μW/cm^2. El trabajo describe los resultados de las mediciones y el análisis del proceso de degradación realizado mediante el estudio de la curva característica densidad de corriente – voltaje (J-V) bajo iluminación LED. Los parámetros de desempeño analizados fueron la PCE, la densidad de corriente de corto circuito (J_{SC}), el voltaje de circuito abierto (V_{OC}) y el factor de llenado (FF). La PCE de los dispositivos encapsulados permaneció por arriba del 80% de su valor inicial después de 624 h.

Introduction

Research in fields related to energy generation has been prominent for decades now because of fossil fuels being scarce and for having a negative impact on the environment, becoming one of the main causes of global warming and air pollution [1] [2]. The interest in finding clean and inexhaustible alternatives has led to the study of different natural resources, like solar energy [3]. However, there are many aspects that need to be investigated for further development, including looking for organic materials capable of substituting silicon as the main active material in photovoltaic cells. One example are semiconducting organic polymers [1], which have advantages like being cheaper, easier to prepare, flexible and lightweight [4].

The problem right now is that organic materials can't display efficiencies comparable to silicon-based cells, and their degradation rates are not satisfying. However, something about organic cells that has attracted the attention of researches lately is their potential for indoor applications.

In recent years the amount of electronic devices has increased exponentially, especially those related to communications that conform the Internet of Things (IoT) [5]. This has motivated the investigation of ways to charge them without relying on batteries [6]. As a result, photovoltaic cells have become interesting for this purpose, seeing that electronic devices like IoT usually demand electrical power in ranges of 1 to 100 mW. This is something possible using solar cells and has directed researchers to new areas of development [7].

The reason why organic solar cells (OSC) are especially interesting for indoor applications is that organic materials have the ability to absorb radiance in the visible region of the light spectrum, ranging from 390 to 760 nm. This matches common artificial light used at offices and areas of very high visual demand, like LEDs [8], which require illuminations of at least 500 or 1000 lux [9]. Studies have proven to really promising, as the use of certain organic materials has led to PCE of over 23% under a 1000 lux LED [10].

Even after those positive results, the stability of the devices is still an unsatisfactory key aspect that stops their possibilities to be commercialized [11]. Encapsulation becomes an especially interesting process to achieve long-term performances by providing protection from external threats, turning into a direct link to the device's stability [12]. In addition, external and internal factors that affect degradation need to be studied to understand the process that takes place at each one of the device's layers [13] [14].

In this project, the evolution of J-V parameters is performed to understand the degradation of conventional polymeric cells, using a copolymer called PTB7:$PC_{70}BM$ as the active layer. Similar materials or structures have been studied in previous works, achieving promising results [15, 16] and making it interesting to investigate other variations. The behavior of the cells is studied under 1000 lux artificial LED 2700 K light, following the consensus stability testing protocols for organic photovoltaic materials and devices [17]. The encapsulated and non-encapsulated cells are kept under controlled environments to see how this affects degradation.

Materials and methods

The conventional structure chosen for this project was the next one: ITO/PEDOT:PSS/ PTB7:$PC_{70}BM$/Ca/Ag. To start the fabrication of the 0.09 cm^2 cell, the ITO-patterned glass substrates were carefully cleaned to remove any possible dust or residue. The deposition of the first layer, PEDOT:PSS, was by spin coating at 4000 rpm for 40 s. After that, the samples were put in a heating plate for 15 min at 150 °C for thermal annealing. The rest of the process was performed inside a glove box under nitrogen environment. The active layer solution was prepared in advance, as it needs to age for 48 hours before spin coating it for 30 s at 750 rpm to get a 100 nm width layer. The next two layers, 25 nm of Ca and 100 nm of Ag, were added applying a thermal evaporation procedure inside a vacuum chamber under high pressure conditions.

Results

Two structures of cells were studied, Figure 1 shows the current density-voltage (J-V) characteristics curves under LED illumination condition of the fabricated OSCs. The encapsulated device displaying an initial power conversion efficiency of 12.0%, which decreased to 9.5% after 625 h. This contrasts with the results obtained with cells stored in air, which started at 9.3% and got to 3.5%.

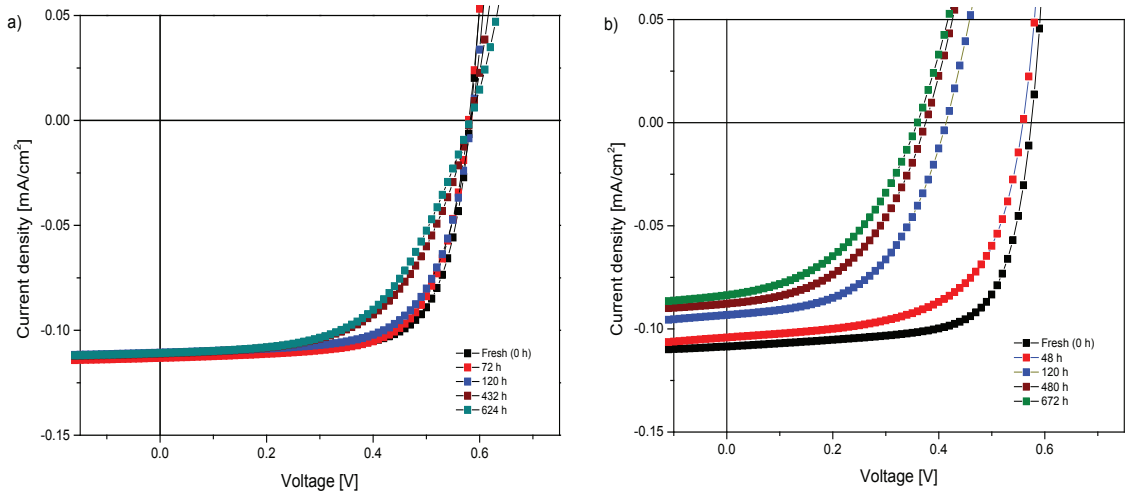

Figure 1. Illuminated J–V curves over time under LED spectrum of OSC based in PTB7:PC70BM a) encapsulated devices, b) non-encapsulated devices.

In addition, the performance parameters (V_{OC}, J_{SC}, PCE, FF) that were obtained from the J–V characterization were normalized with respect to the initial values (Figure 2). This normalization displays how these values drastically decrease in the air stored cells, in which efficiency goes down in a 55% during the first 100 h, getting to lose 70% in about 500 hours. On the other hand, both V_{OC} and FF go down in a 25%, decreasing until the 60% at 500 hours. J_{SC} is the parameter with less changes, decreasing first 15% and then staying mostly stable, ending in the 80%. In contrast, encapsulated cells only see a gradual decrease in FF and PCE parameters, getting down to an 80% after 600 hours, while V_{OC} and J_{SC} stay mostly stable, barely losing a 5% of its initial values. This confirms the positive consequences of applying an encapsulation thanks to the protection of the cells from extrinsic factors like oxygen, and water [14]. While that, the non-encapsulated cells were faster degraded because of being affected by both extrinsic and intrinsic factors which easily degrade organic cells' active layer. Research have concluded that their main degradation cause is UV irradiation because it alters both carrier mobility and the recombination process that creates current, leading to the decrease of PCE between other characteristic parameters [18].

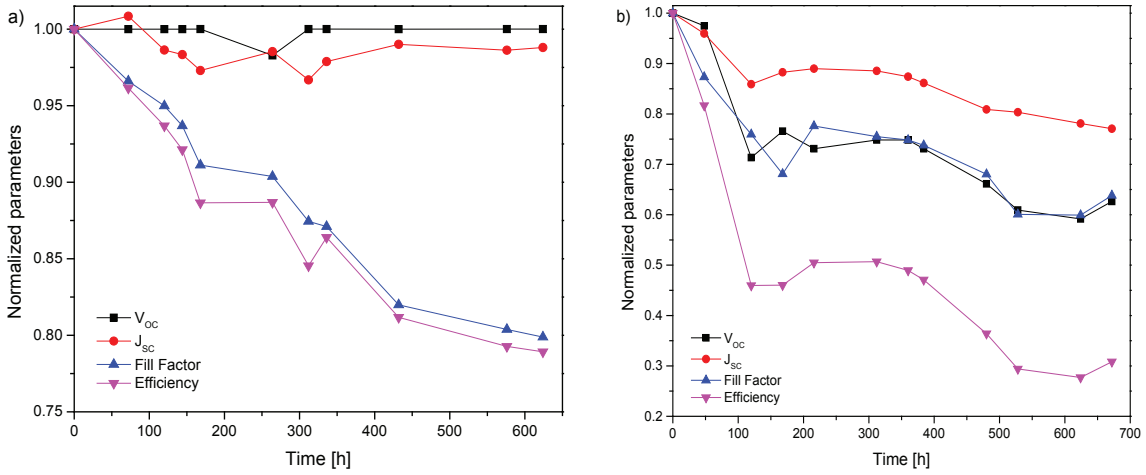

Figure 2. Comparison of the normalized performance parameters (V_{OC}, J_{SC}, FF and PCE) of the OSC during the degradation over time of 650 h a) encapsulated devices, b) non-encapsulated devices.

Conclusion

A first study on the degradation of conventional polymer:fullerene OSC based on PTB7:$PC_{70}BM$ can be performed thanks to the analysis of J-V characteristics. During the first 150 h there is a fast decrease in several parameters, which is known as “burn-in loss”. This can be seen during the first 100 h, especially in the non-encapsulated devices, after which there is a slower degradation. The biggest difference is in PCE, decreasing a 70% in non-encapsulated devices after almost 700 h, while encapsulated ones only dropped around a 20%, confirming the importance of applying encapsulation to OSC to achieve better stability

Acknowledgment

This work was supported by Ministerio de Ciencia e Innovación under Grant PDI2021-128342OB-I00; Diputació de Tarragona under Grant 2021CM14 and 2022PGR-DIPTA-URV04; the Spanish Ministry of Science and Innovation (MICINN/FEDER) under Grant RTI2018-094040-B-I00; the Agency for Management of University and Research Grants (AGAUR) under ref. 2017-SGR-1527

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Analyzing the Stability of Organic Photovoltaic under Indoor illumination

Marta Serantes[1], Magaly Ramírez-Como[1], Enas Moustafa[1], Alfonsina Abat Amelenan Torimtubun[1], Lluis F. Marsal[1], Josep Pallarès[1]

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Introduction

Research related to energy generation has been prominent for decades now, leading to the study of clean and inexhaustible sources like solar energy. This field has many possibilities, including the use of semiconducting organic polymers instead of silicon as active materials.

In addition, the use of organic materials has big potential for indoor applications thanks to their ability to absorb radiance in the visible region of light spectrum, matching common artificial light. However, these cells don't have good enough efficiencies, stability and degradation rates.

Encapsulation becomes an important process to achieve long-term performance, providing protection from external threats.

Behavior analysis.
Evolution of J-V parameters to understand cell's degradation.
Analysis under 1000 lux artificial LED 2700 K light.

Materials and Methods

Preparation of conventional PTB7: $PC_{70}BM$ polymer cells.
ITO/PEDOT:PSS/PTB7:$PC_{70}BM$/Ca/Ag - 0.09 cm^2

1) Polymer solution preparation - Aging for 48 h.
2) Clean ITO-patterned glass substrates.
3) PEDOT:PSS deposition (spin coating at 4000 rpm for 40 s).
4) Annealing at a heating plate for 15 min at 150 °C.
5) PTB7:$PC_{70}BM$ deposition (spin coating for 30 s at 750 rpm).
6) Ca deposition (thermal evaporation under high pressure).
7) Ag deposition (thermal evaporation under high pressure).
8) Optical Adhesive encapsulation.

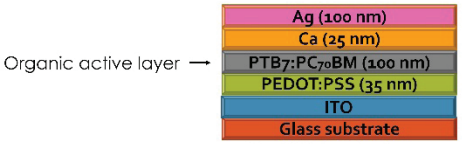

Fig. 1 Cell's structure.

Results and Discussion

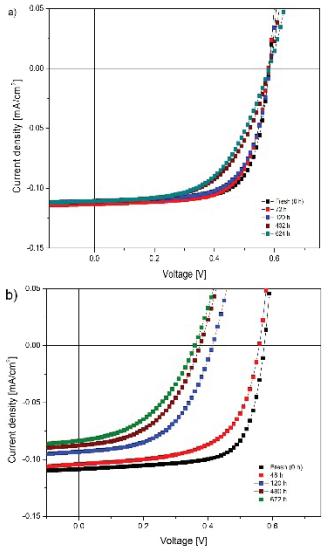

Fig. 2 . Illuminated J–V curves over time under LED illumination a) encapsulated cells, b) non-encapsulated cells.

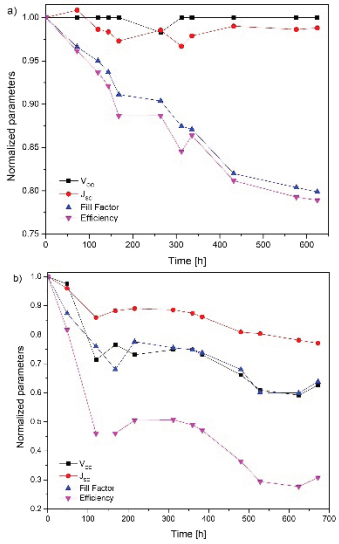

Fig. 3 . Comparison of normalized performance parameters over 650 h a) encapsulated cells, b) non-encapsulated cells.

Conclusions

- During the first 150 h there is a fast decrease in several parameters, which is known as "burn-in loss".
  Burn-in losses appear especially during the first 100 h in non-encapsulated devices.
- The biggest difference is in PCE.
  Decreases a 70% in non-encapsulated devices after almost 700 h, while encapsulated cells remained close to 80%.
- In encapsulated cells the fill factor decreases in a similar way to the efficiency, while Voc and Jsc barely change.
- In non-encapsulated cells fill factor and Voc both decrease in a similar manner, ending at a 70% while Jsc stays at 80%.
- **Confirmation of the importance of OSC's encapsulation to achieve better stability.**

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Illustration 1. Presented Poster at LAEDC 2022.

Analysis of the degradation of high-efficiency encapsulated PM6:Y7-based Photovoltaic Cells

Análisis de la degradación de celdas fotovoltaicas encapsuladas de alta eficiencia basadas en PM6:Y7

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Keywords

Degradation Analysis; PM6:Y7; organic solar cells; no fullerenes acceptor; encapsulated cells.

Abstract

In this work, we report a degradation study of high-efficiency conventional polymer solar cells (PSCs). The high performance of the PM6:Y7-based device is achieved with a power conversion efficiency (PCE) of up to 15.64% in the first measurement. The article describes the results of the measurements and analysis of the degradation process. The electrical parameters during the degradation process were extracted from the current density – voltage characteristics curves (J–V) under light and dark conditions. Were observed the specific parameters of the selected cells: open-circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), PCE, series (R_S), and shunt (R_{SH}) resistance values The PCE of the device decreased down to 64% of the initial PCE after 1056 h.

Resumen

En este trabajo, nosotros reportamos un estudio de celdas solares poliméricas (PSCs) convencionales de alta eficiencia. El alto desempeño del dispositivo basado en PM6:Y7 se logró con una eficiencia de conversión de potencia (PCE) de hasta el 15.64 % en la primera medición. El artículo describe los resultados de las mediciones y el análisis del proceso de degradación. Los parámetros eléctricos durante el proceso de degradación fueron extraídos de las curvas características de densidad de corriente-voltaje (J–V) en condiciones de luz y bajo oscuridad. Se observaron los parámetros específicos de las celdas seleccionadas: voltaje de circuito abierto (V_{OC}), densidad de corriente de cortocircuito (J_{SC}), factor de llenado (FF), PCE, serie (R_S) y resistencia en paralelo (R_{SH}). La PCE del dispositivo disminuyó hasta el 64% del su PCE inicial después de 1056 h.

Palabras clave

Análisis de degradación; PM6:Y7; celdas solares orgánicas; aceptores no fulerenos; celdas encapsuladas.

Introduction

Today's developments in organic solar cells allow us to look to the future of the field with hope. Polymer Solar Cells (PSCs) are attracting attention due to their light weight and low cost, as well as their ability to be manufactured on a large-scale using roll-to-roll technology. The materials used as the electron transport layer (ETL) and hole transport layer (HTL) play an important role in the electrical performance of the device [1-4]. In this text, we would like to present the results of research on conventional PSC fabricated were based on the structure of ITO/PEDOT:PSS/PM6:Y7/PDINO/Ag carried out during 1056 hours.

Materials and methods

Conventional PSC fabricated were based on the structure of ITO/PEDOT:PSS/PM6:Y7/PDINO/Ag as shown in Figure 1(a). Firstly, the ITO glass substrates were cleaned. Then the PEDOT:PSS solution was deposited on top of the precleaned ITO substrates at 4000 rpm for 40 s and then annealed in the air for 15 min at 150 °C. The active layer PM6:Y7 blend with the weight ratio of 1:1 was dissolved in chlorobenzene (CB) and 1-chloronapthalene (CN), (CB:CN = 99.5:0.5

by volume). The blend solution was spin-coated onto the ITO/PEDOT:PSS substrates to obtain an active layer thickness of around 100 nm. Afterward, the electron transport layer, PDINO was deposited by spin coating at 3000 rpm for 30 s, obtaining a thickness of 35 nm. Then was evaporated at 100 nm Ag under high vacuum conditions. The effective area of the devices was 0.09 cm^2.

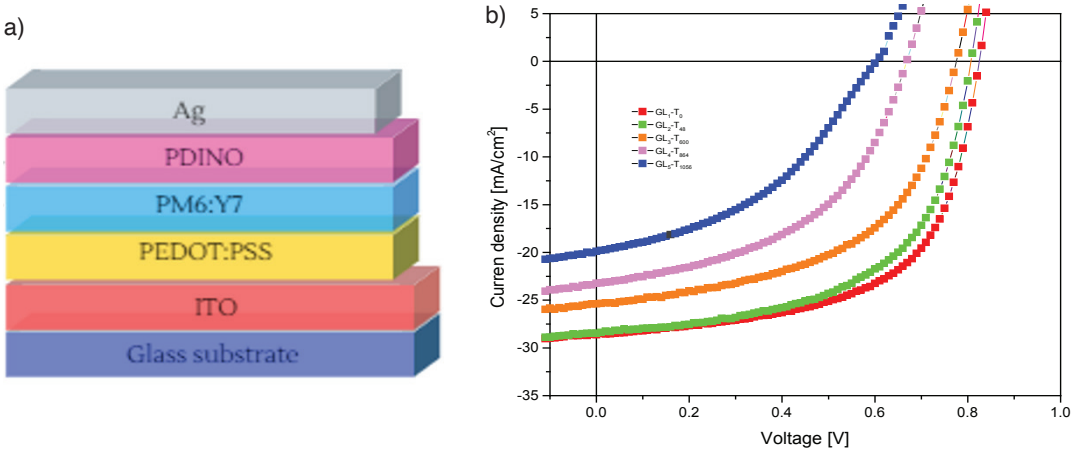

Figure 1. (a) Conventional architecture of the fabricated based in PM6:Y7. (b) Illuminated J–V curves over time under AM 1.5G spectrum.

Results

In this part of the work, we study to analyze the performance and the stability of PSCs. The current density-voltage (J-V) characteristics of the devices under light (Figure 1b) and dark (Figure 2b) were performed at room temperature using a Keithley 2400 source measure 100 mW/cm^2 and AM1.5G spectrum. The encapsulated devices were analyzed under an air environment for up to 1056 h. Figure 1(b) shows illumination the current density-voltage (J-V) characteristics curves under illumination condition and performance of the freshly prepared samples, GL1-T0, and after the photo-aging test: GL2-T48 (48 hours after the first measurement), GL3-T600, GL4-T864, up to GL5-T1056 (1056 hours after the first measurement). It can be observed that the J – V curve for the degraded cell under AM 1.5G illumination (Figure 1b) was shifted to lower open-circuit voltage (V_{OC}) like as [5,6,9].

Moreover, Table I shows the specific parameters of the selected cells: open-circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), power conversion efficiency (PCE), series (R_S), and shunt (R_{SH}) resistance values. Where the PCE, V_{OC}, J_{SC}, FF values were reduced from 14.2%, 820mV, 28.6 mA/cm2, 0.60 at T0 to 5.1%, 600 mV, 19.9 mA/cm2, 0.42, at T1056. Figure 2(a) shows full graphs of all measurements for which selected data are shown in Table 1. The normalized performance parameters detailed that have been investigated over time until reaching T1056.

Table 1. Performance parameter for the fabricated PSC.

Sample	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF	PCE (%)	R_S (Ωcm^2)	R_{SH} (Ωcm^2)
Fresh T0 h	820	28.6	0.60	14.2	1.77	324
T48 h	810	29.2	0.65	13.1	1.82	210
T600 h	780	25.4	0.53	10.5	2.65	203
T864 h	670	23.2	0.49	7.6	3.66	139
T1056 h	600	19.9	0.42	5.1	7.79	115

In Figure 2(a), the cells show a first, faster decay of PCE (approximately 7% of the starting value) in the initial hours from 0 h to 48 h. This atrophy is generally described as one of the degradation damage mechanisms, which is known as “burn-in loss”[7, 8]. Subsequently, in the case of PCE, we can observe a sudden increase and a renewed downward trend. Beyond 408 h we can then observe only decreasing trends. Other the performance parameter to be taken into account is FF, as shown in Figure 2(a). The normalized FF in solar-aged devices decreases rapidly by about 11% of the initial value up to 96 h. The value then returns to a value of 98% of the initial value and gradually decreases.

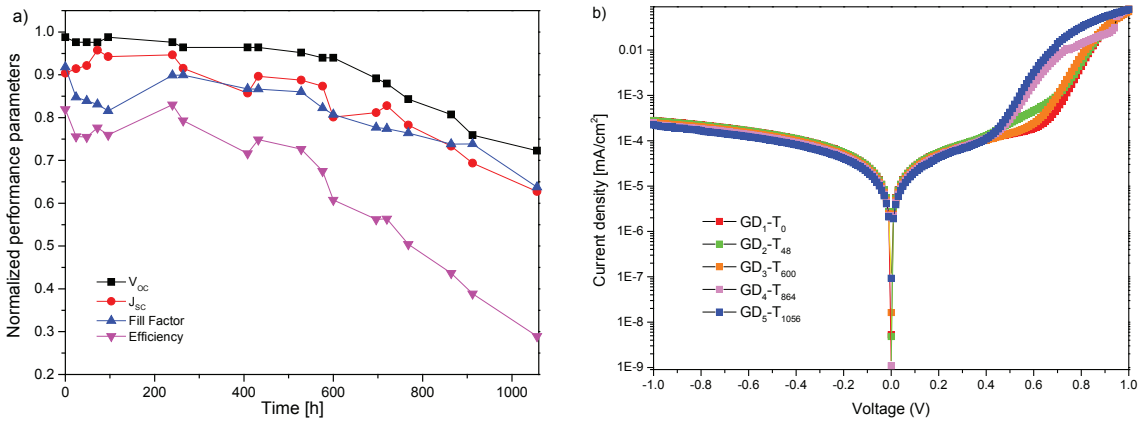

Figure 2. (a) Comparison of the normalized performance parameters (V_{OC}, J_{SC}, FF, and PCE) of the degradation over time of 1056 h. (b) J-V curves over time under dark.

Figure 2(b) shows the J-V characteristic curves produced under dark conditions. It is clear that there is a gradual small increase in leakage current. This agrees with the gradual decrease in shunt resistance (Table 1).

Conclusion

The stability of high efficiency conventional PSC based on bulk heterojunction PM6:Y7 can be investigated by analysis of the current density-voltage (J-V) characteristics. The encapsulated PM6:Y7 devices presents a fast decrease in the first hours that is known as “burn-in loss”. However, the PCE of the devices remained over 30% after 1056 h. Therefore, the solar cells PM6:Y7 based is a promising structure that could be use in the future to scaling up the PSC. To better understand the degradation behavior of the cells were measure with the impedance spectroscopy. Therefore, the next work is to continue with the analysis of this measurements.

Acknowledgment

This work was supported by Ministerio de Ciencia e Innovación under Grant PDI2021-128342OB-I00; Diputació de Tarragona under Grant 2021CM14 and 2022PGR-DIPTA-URV04; the Spanish Ministry of Science and Innovation (MICINN/FEDER) under Grant RTI2018-094040-B-I00; the Agency for Management of University and Research Grants (AGAUR) under ref. 2017-SGR-1527.

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Analysis of the degradation of high-efficiency encapsulated PM6:Y7-based Photovoltaic Cells

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Introduction

Photovoltaic Solar Cells (PSCs) are attracting attention due to their lightweight and low cost, as well as their ability to be manufactured on a large scale using roll-to-roll technology. The materials used as the electron transport layer (ETL) and hole transport layer (HTL) play an important role in the electrical performance of the device.

Materials and Methods

Conventional PSC structure of ITO/PEDOT:PSS/PM6:Y7/PDINO/Ag

1. ITO glass substrates were cleaned
2. PEDOT:PSS solution was deposited on top of substrates at 4000 rpm for 40 s, annealed in the air for 15 min at 150 °C.
3. PM6:Y7 blend with the weight ratio of 1:1 was dissolved in chlorobenzene (CB) and 1-chloronapthalene (CN), (CB:CN = 99.5:0.5 by volume).
4. The blend solution was spin-coated onto the ITO/PEDOT:PSS (+/-100 nm).
5. PDINO was deposited by spin coating at 3000 rpm for 30 s (35 nm) and evaporated at 100 nm Ag under high vacuum conditions.
6. The effective area 0.09 cm^2.

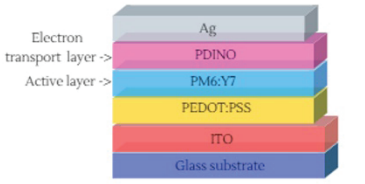

Fig. 1 Conventional architecture of the fabricated based in PM6:Y7.

Results and Discussion

Table I the specific parameters of the selected cells: open-circuit voltage (V_{OC}), short circuit current density (J_{SC}), fill factor (FF), power conversion efficiency (PCE), series (R_S), and shunt (R_{SH}) resistance values.

Sample	V_{OC} (mV)	J_{SC} (mA/cm^2)	FF	PCE (%)	R_S (Ωcm^2)	R_{SH} (Ωcm^2)
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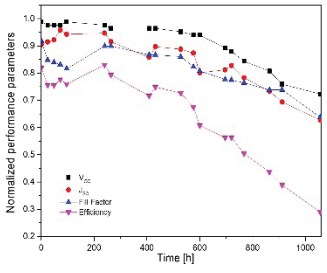

Fig. 2 Comparison of the normalized performance parameters (V_{OC}, J_{SC}, Fill Factor and Efficiency) of the degradation over time of 1056 h.

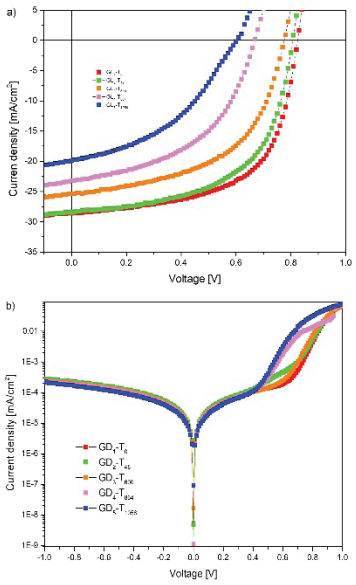

Fig. 3 (a) Illuminated density-voltage (J-V) characteristics **(b)** under dark. Were performed at room temperature using a Keithley 2400 source measuring 100 mW/cm^2, under an air environment and time 1056 h.

Conclusions and Next Steps

- The stability of high efficiency conventional PSC based on bulk heterojunction PM6:Y7 can be investigated by analysis of the current density-voltage (J-V) characteristics.
- The encapsulated PM6:Y7 devices present a fast decrease in the first hours which is known as "burn-in loss".
- PCE of the devices remained over 30% after 1056 h.
- Is planning, to better understand the degradation, implementation of measurements spectroscopy.

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Illustration 1. Presented Poster at LAEDC 2022.

Emerging 2D materials for tunneling field effect transistors

Materiales 2D emergentes para transistores de efecto de campo de efecto túnel

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Navlakha, N; Register, L.F; Banerjee, S.K. Emerging 2D materials for tunneling field effect transistors. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 72-78.

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Keywords

Tunnel field effect transistor; transitional metal dichalcogenides; type-III band alignment; heterostructure; black phosphorus; group IV Monochalcogenides.

Abstract

This work focuses on understanding the electronic properties of materials to enhance the performance of Tunnel Field Effect Transistor (TFET) through Density Functional Theory (DFT) simulations. Material selection prefers a *p*-type material with in-plane high density of state (DOS) (and low out-of-plane effective mass, m^*, where defined for many layer systems), and high valence band maxima (VBM) energy stacked with an *n*-type material with low conduction band minimum (CBM) energy (large electron affinity (EA)) that creates a broken or nearly broken band alignment and has low lattice mismatch. $SnSe_2$ is well-suited for an *n*-type 2D material due to high EA, while WSe_2, Black phosphorous (BP) and SnSe are explored for *p*-type materials. Bilayers consisting of monolayers of WSe_2 and $SnSe_2$ show a staggered but nearly broken band alignment (gap of 24 meV) and a high valence band DOS for WSe_2. BP-$SnSe_2$ shows a broken band alignment and benefits from a low lattice mismatch. SnSe-$SnSe_2$ shows the highest chemical stability, an optimal performance in terms of DOS of SnSe, tunability with an external field, and high VBM that also leads to a broken band alignment.

Palabras clave

Transistor de efecto de campo de túnel; dichaslcogenuros de metales de transición; alineación de bandas de tipo III; heteroestructura; fósforo negro; monocalcogenuros del grupo IV.

Resumen

Este trabajo se centra en comprender las propiedades electrónicas de los materiales para mejorar el rendimiento del transistor de efecto de campo de túnel (TFET) a través de simulaciones de la teoría funcional de la densidad (DFT). La selección de material prefiere un material de tipo *p* con alta densidad de estado (DOS) en el plano (y baja masa efectiva fuera del plano, m^*, donde se define para muchos sistemas de capas), y alta energía máxima de banda de valencia (VBM) apilado con un material de tipo *n* con energía mínima de banda de conducción baja (CBM) (afinidad electrónica grande (EA)) que crea una alineación de banda rota o casi rota y tiene un desajuste de red bajo. $SnSe_2$ es muy adecuado para un material 2D de tipo *n* debido a su alta EA, mientras que WSe_2, fósforo negro (BP) y SnSe se exploran para materiales de tipo *p*. Las bicapas que consisten en monocapas de WSe_2 y $SnSe_2$ muestran una alineación de bandas escalonada pero casi rota (brecha de 24 meV) y un DOS de banda de alta valencia para WSe_2. BP-$SnSe_2$ muestra una alineación de banda rota y se beneficia de un desajuste de red bajo. SnSe-$SnSe_2$ muestra la mayor estabilidad química, un rendimiento óptimo en términos de DOS de SnSe, sintonizabilidad con un campo externo y VBM alto que también conduce a una alineación de banda rota.

Introduction

2D-materials based Tunnel Field Effect Transistors (TFET) facilitate high interlayer tunneling on-currents (I_{on}) and gate controllability for short lateral channel lengths [1-6]. Although, graphene, transitional metal dichalcogenides (TMD), and their lateral and vertical heterostructures [2] have been investigated widely for TFETs [1,3,4], optimization to improve device design, reduce the off-current (I_{off}), improve I_{on} and sub-threshold swing (*SS*) and off current (I_{off}) is still needed.

Recently, WSe_2-$SnSe_2$ has shown promising results for vertical TFETs [5]. Moreover, WSe_2 shows ambipolar characteristics and can be replaced with a *p*-type material [1,3]. Use of a vertical hetero-bilayer that forms a broken or near broken band gap and requires less strain to form a lattice matched supercell is advantageous [3,4]. Here we explore other heterostructures for possible TFET application through Density Functional Theory (DFT) and compare results with those for WSe_2-$SnSe_2$. Results suggest that BP [7] and SnSe [8] can substitute for the *p*-type material in TFETs and is benefited with a higher strain tolerance, as well offer potential optoelectronics applications.

Computational method

Our calculations are performed using DFT with the projector-augmented wave method as implemented using the Vienna Ab initio Simulation Package [9]. The exchange-correlation interaction is included using the generalized gradient approximation developed by Perdew-Burke-Ernzerhof [10]. The lattice parameters of monolayers are optimized, and the calculated band gaps are consistent with previous literature [2,7,8,11]. The van der Waals (vdW) interactions are modeled using the OptB88 method [12]. The structures were fully relaxed with a force tolerance of 0.01 eV/Å. The energy cutoff was 400 eV, and the break criterion for the electronic self-consistent loop was 10^{-5} eV.

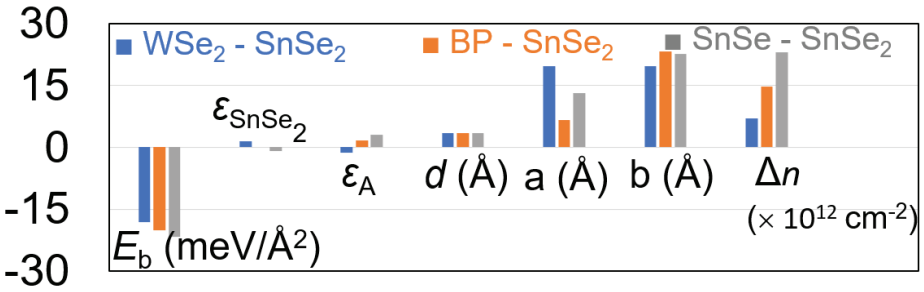

Figure 1. Comparison of binding energy per unit area (E_b), strain applied to create heterostructure (where ε and ε_A is the maximum strain applied in either *x* and *y* for $SnSe_2$, and material A (WSe_2, BP, SnSe), respectively, optimal interlayer distance (*d*), the dimensions of the lattice supercell created in the *x* (*a*) and *y* (*b*) directions, all in units of angstroms (Å), electron concentration (Δn) redistributed from Material A to $SnSe_2$ at zero applied field, in the heterolayers of WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$.

Results and discussion

Enhancing I_{on} requires a high Density of States (DOS) 2D material with high Valence Band Maxima (VBM) as the *p*-type material and an *n*-type material with a low Conduction Band Minima (CBM) or large Electron Affinity (EA) [3]. $SnSe_2$ shows high EA, while BP, WSe_2 and SnSe show a high VBM energy. We compare heterostructures of WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$. The binding energy per unit area (E_b) between the layers is calculated as $E_b = (E_{A/SnSe_2} - E_A - E_{SnSe_2})$ divided by the simulated heterostructure area, where $E_{A/SnSe_2}$, E_A, and E_{SnSe_2} are the total energy of the heterostructure, material A (WSe_2, BP, or SnSe), and $SnSe_2$, respectively, and Area is a ´ b, as defined in Fig. 1. The interlayer separation, *d*, is calculated as that which maximizes the magnitude of the (intrinsically negative) interlayer binding energy E_b, both provided Fig. 1. And the greater the magnitude of E_b, the more stable the structure. SnSe-$SnSe_2$, is the most stable followed in order by BP-$SnSe_2$ and WSe_2-$SnSe_2$. The lattice mismatch is the least for BP-$SnSe_2$ (1.6% in *y*-direction, zigzag and 0.3% in *x*, armchair)

and most for SnSe-$SnSe_2$ (-1% for $SnSe_2$, 2.9% in the *y*-direction of SnSe) (Fig. 1). Mismatch can result in disorder, which is difficult to control during fabrication and can impact the interlayer coupling [5]. However, the maximum strain in each layer is less than 3%.

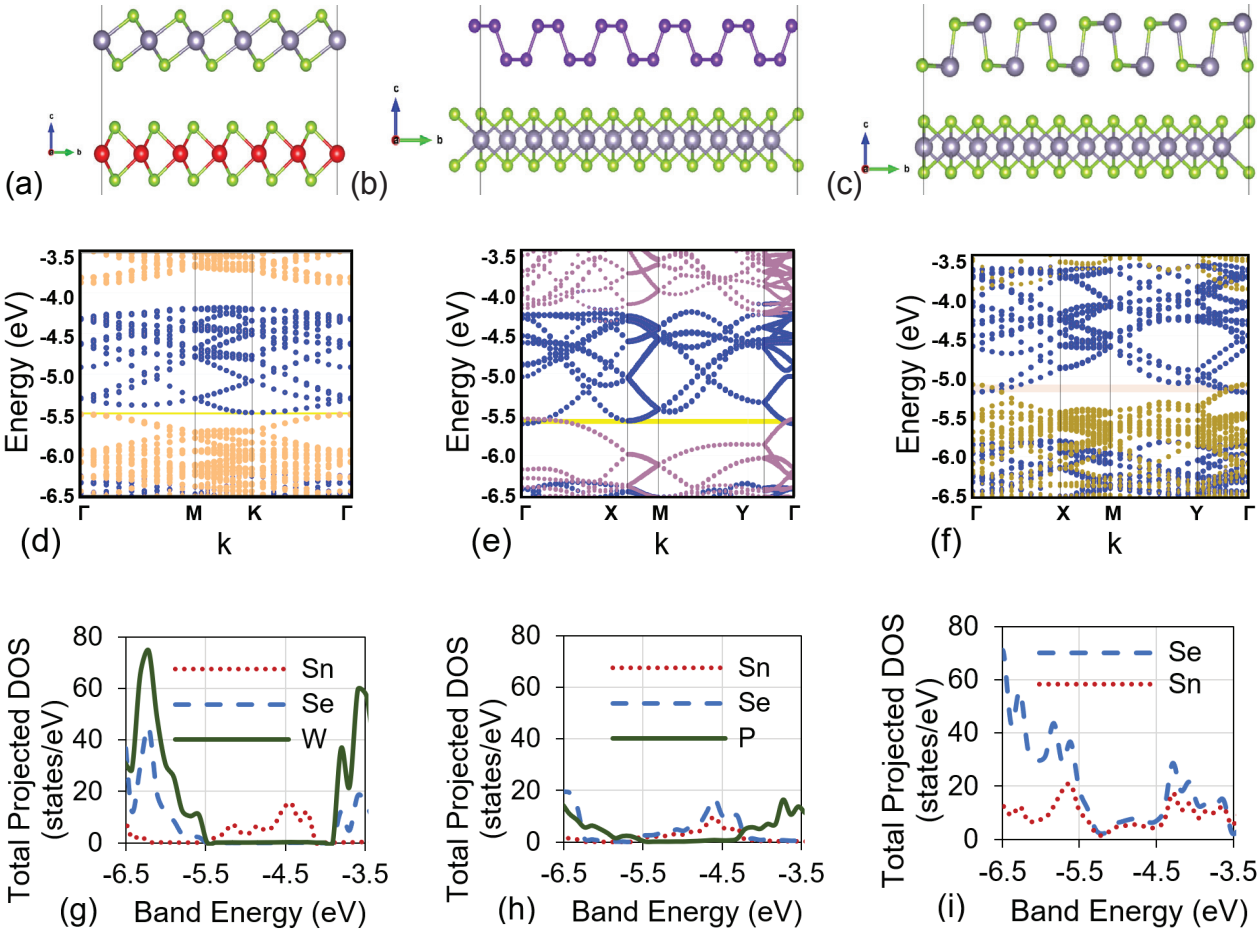

Figure 2. (a-c) The crystal structure in the *y-z* plane, (d-f) projected band structure, and (g-i) total projected density of state (DOS) of each material for WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$ in sequence. In (d-f), $SnSe_2$,WSe_2, BP, and SnSe atoms are represented in blue, cream, purple, green, respectively. All energies are referenced to vacuum level.

We stacked a 5x5, a √3x6, and a 2 √3x6 supercell of $SnSe_2$ with a 6x6 supercell of WSe_2, a 2x5 supercell of BP, and a 3x5 supercell of SnSe, respectively. (Fig. 2(a)-(c), respectively), resulting in supercells with dimensions shown in Fig. 1. The Bader charge analysis was used to obtain the electron redistribution from WSe_2, BP, and SnSe, which are 7.0 x 10^{12} cm^{-2}, 1.5 x 10^{13} cm^{-2} and 2.3 x 10^{13} cm^{-2}, respectively (Fig. 1). This charge transfer between the layers results in electrostatic interlayer coupling, which contributes to the aforementioned interlayer binding energy. Fig. 2 (d)-(f) shows that the CBM of each heterostructure originates from $SnSe_2$ and the VBM from material A. Fig. 2(d) shows the resulting Type II alignment for WSe_2-$SnSe_2$ with heterostructure band gap E_g = 24 meV, which can be tuned to a Type III alignment with a small potential. A Type III alignment is found for BP-$SnSe_2$ and SnSe-$SnSe_2$ with an overlap of the conduction and valence bands of 21 meV (Fig. 2(e)) and 31 meV (Fig. 2(f)), respectively. Fig. 2(g)-(i) shows the total atom-projected DOS for each material. The valence band DOS near the band-edge is highest for WSe_2-$SnSe_2$, still comparable for SnSe-$SnSe_2$, while that for BP-$SnSe_2$ is substantially smaller.

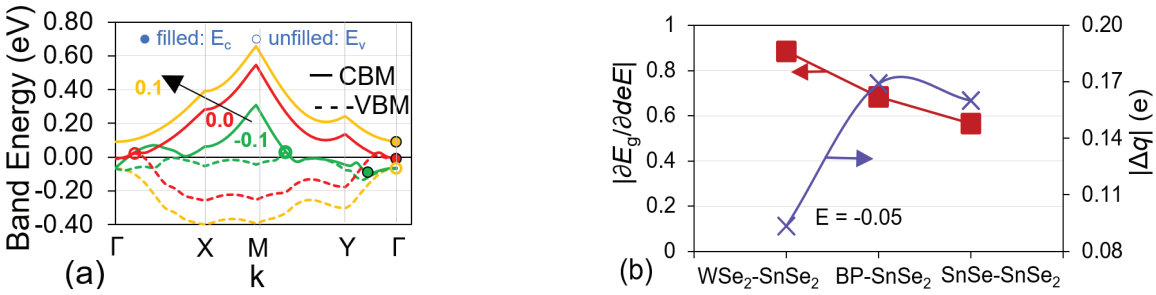

Figure 3. (a) The variation in the band structure associated with the CBM and VBM for SnSe-$SnSe_2$ with Electric field, *E* (-0.1 V/Å, 0.0 V/Å, 0.1 V/Å). All energies in (a) are referenced to DFT supplied fermi level. (b) Variation in band gap E_g with applied external electric field *E* (-0.05 V/Å) adjusted for the interlayer separation *d* and electron charge magnituded *e*, $|\partial E_g/\partial(deE)|$ and the change in electron distribution (Δq) in Material A (opposite that in $SnSe_2$) due to an an applied external electric field of *E* of -0.05 V/Å. Note that in the absence of field screening within the the bilayer, $|\partial E_g/\partial(deE)|$ would be approximately unity.

Minimizing the sub-threshold swing requires maximizing gate efficiency, which can be quantified as change in the band overlap with applied voltage [13], where a higher change in E_g with a lower bias is desirable. The impact of external field on the band alignment can be observed in Fig. 3(a), where a positive field is directed from Material A to $SnSe_2$. For a 0.1 V/Å, SnSe-$SnSe_2$ shows a Type-II band alignment with a direct band gap. We compared the change in band gap with a field of –0.05 V/Å, which is equivalent to an interlayer potential difference of ~0.17 V between the layers for each heterostructure. Fig. 3(b) shows the variation is maximum for WSe_2-$SnSe_2$, followed by BP-$SnSe_2$, and SnSe-$SnSe_2$. The change in the charge distribution with applied external field is the largest for BP-$SnSe_2$. This result shows a possibility for better current control for this heterostructure as compared to the others. The material requirements and the results obtained here suggest SnSe-$SnSe_2$ could be utilized as a channel material for TFETs. Other Group-IV monochalcogenides [8] also could be explored as the *p*-type material for TFETs.

Conclusion

The work emphasizes on the need to replace the devices with new material system. The objective is to explore $SnSe_2$ heterostructures that can operate as tunneling transistors. Comparing WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$ shows that SnSe-$SnSe_2$ provides optimal performance in terms of stable structure, high DOS, tunability with electric field, and a broken band alignment that nominates it for being investigated at device level.

Acknowledgment

We thank National Nanotechnology Coordinated Infrastructure (NNCI), which is supported by the National Science Foundation under the Grant ECCS-2025227. We also acknowledge the Texas Advanced Computing Center (TACC) at The University of Texas at Austin for providing high performance computing resources for this work.

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Emerging 2D Materials for Tunneling Field Effect Transistors

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Introduction

2D material based heterostructure as Vertical Tunnel Field Effect Transistor (TFET), FIG. 1:

- High interlayer tunneling on-currents (I_{on}) and gate controllability
- Non-dangling bond reduces the performance degradation occurring due to traps in lateral heterojunction based TFETs
- Need new material systems for enhanced performance

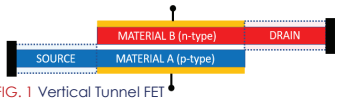

FIG. 1 Vertical Tunnel FET

Material requirement/selection for enhanced performance:

- Bilayer with a near broken or broken band gap
- Requires less strain to form a lattice matched supercell
- High Density of States (DOS) 2D material with high Valence Band Maxima (VBM) energy as the *p*-type material
- *n*-type material with a low Conduction Band Minima (CBM) energy or large Electron Affinity (EA)

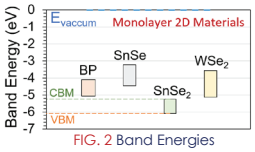

FIG. 2 Band Energies

Material selection (FIG. 2)
$SnSe_2$: High EA (*n*-type)
WSe_2, SnSe, BP : High VBM (*p*-type)
Bilayers for comparison:
WSe_2 - $SnSe_2$, BP - $SnSe_2$, SnSe - $SnSe_2$

Materials and Methods

- Density Functional Theory (DFT) calculations performed using Vienna Ab initio Simulation Package (VASP).
- Projector-augmented wave (PAW), Exchange-correlation interaction - Generalized Gradient Approximation (GGA) developed by Perdew-Burke-Ernzerhof (PBE)
- van der Waals interactions - OptB88 functional method

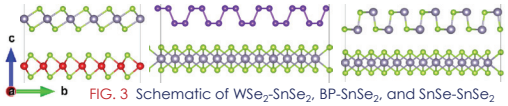

FIG. 3 Schematic of WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$

- Stacked a 5×5, a √3×6, and a 2√3×6 supercell of $SnSe_2$ with a 6×6 supercell of WSe_2, a 2×5 supercell of BP, and a 3×5 supercell of SnSe, respectively (FIG. 3).

Results and Discussion

- Greater the magnitude of E_b, more stable the structure. Stability: SnSe-$SnSe_2$ > BP-$SnSe_2$ > WSe_2 -$SnSe_2$ (FIG. 4).
- Lattice mismatch: SnSe-$SnSe_2$ > WSe_2 -$SnSe_2$ > BP-$SnSe_2$
- Higher charge transfer between layers → better interlayer coupling: SnSe-$SnSe_2$ > BP-$SnSe_2$ > WSe_2 -$SnSe_2$

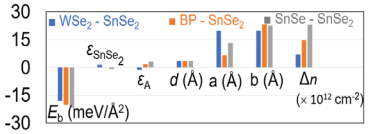

FIG. 4 Parameters of WSe_2-$SnSe_2$, BP-$SnSe_2$, and SnSe-$SnSe_2$ bilayers
1. Binding energy per unit area (E_b), $E_b = (E_{A/SnSe_2} - E_A - E_{SnSe_2})$, 2. Strain applied to create heterostructure (where ε and ε_A is the maximum strain applied in either x and *y* for $SnSe_2$, and material A (WSe_2, BP, SnSe), respectively, 3. Optimal interlayer distance (*d*), 4. The dimensions of the lattice supercell created in the x (*a*) and *y* (*b*) directions, all in units of angstroms (Å), 5. Electron concentration (Δn) redistributed from Material A to $SnSe_2$ at zero applied field.

- Type II alignment for WSe_2-$SnSe_2$ with heterostructure band gap E_g = 24 meV (FIG. 5(a))
- Type III alignment for BP-$SnSe_2$ with an overlap of 21 meV of the conduction and valence bands (FIG. 5(b))
- Type III alignment for SnSe-$SnSe_2$ with an overlap of 31 meV of the conduction and valence bands (FIG. 5(c)).

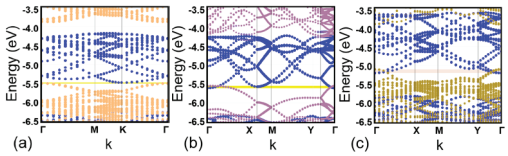

FIG. 5 Band Energies of (a) WSe_2-$SnSe_2$, (b) BP-$SnSe_2$, and (c) SnSe-$SnSe_2$

- The valence band DOS near the band-edge is highest for WSe_2-$SnSe_2$, still comparable for SnSe-$SnSe_2$, while that for BP-$SnSe_2$ is substantially smaller (FIG. 6).
- Analysis with an external field shows tunability in all bilayers

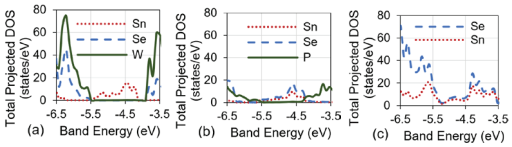

FIG. 6 Projected DOS for (a) WSe_2-$SnSe_2$, (b) BP-$SnSe_2$, and (c) SnSe-$SnSe_2$

Conclusions / Next Steps

- Properties of bilayer material system with nearly broken or broken band gap are compared for TFET operation where,
- WSe_2 -$SnSe_2$ is beneficial due to high DOS and tunes into a broken band gap with a small external field
- BP- $SnSe_2$ has low lattice mismatch
- SnSe-$SnSe_2$ provides optimal performance in terms of most stable structure, high DOS, band tunability with electric field
- SnSe-$SnSe_2$ shows potential to investigate at device level.
- Other Group IV Monochalcogenides can be explored as *p*-type material in TFET device.

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Illustration 1. Presented Poster at LAEDC 2022.

An 8-bit TDC implemented with two nested Johnson counters

Un TDC de 8 bits implementado con dos contadores Johnson anidados

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Santiago-Fernandez, J; Diaz-Sanchez, A; Zamora-Mejia, G; Rocha-Perez, J. M. An 8-bit TDC implemented with two nested Johnson counters. *Tecnología en Marcha*. Vol. 36, special issue. June, 2023. IEEE Latin American Electron Devices Conference (LAEDC). Pág. 79-87.

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Keywords

TDC; Jonhson counter; semi-dynamic logic; nested counters; time-lapse measurement; time-to-digital converter.

Abstract

This work presents a Time-to-Digital Converter implemented using two nested Johnson counters and suitable for time-lapse measurement applications. The proposed structure is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a single decoder. Semi-dynamic logic was used for the decoder to reduce its power consumption. The system has a standard digital output and is powered by a 1.8 V supply with a total power consumption of 32.4 mW. A prototype was fabricated using a TSMC 180 nm CMOS technology. The proposed structure uses a 508 µm x 225 µm area. In addition, this TDC has a standard deviation of 0.78 LSB with a fixed input time interval operating at a frequency of 1 MHz. The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC.

Palabras clave

TDC; contador Johnson; lógica semi-dinámica; contadores anidados; mediciones de intervalo de tiempo; convertidor de tiempo a digital.

Resumen

Este trabajo presenta un Convertidor de Tiempo a Digital implementado utilizando dos contadores Johnson anidados y apropiado para aplicaciones de medición de intervalo de tiempo. La estructura propuesta se compone de dos contadores anidados de 4 bits, dos redes de control lógico-digital, dos registros y un decodificador. Para el decodificador se ha utilizado una lógica semi-dinámica para reducir su consumo de energía. El sistema tiene una salida digital estándar y se alimenta con una fuente de 1.8 V con un consumo total de 32.4 mW. Se fabricó un prototipo utilizando una tecnología CMOS de 180 nm de TSMC. La estructura propuesta ocupa un área de 508 µm x 225 µm. Además, este TDC tiene una desviación estándar de 0.78 LSB con un intervalo de tiempo de entrada fijo que opera a una frecuencia de 1 MHz. La estructura propuesta muestra buenos resultados de rendimiento y repetibilidad para condiciones de conversión continua, estos resultados son atribuidos a la simplicidad del sistema y al uso de contadores con mínimo retardo de puerta como elementos principales para el TDC.

Introduction

The channel length reduction and node scalling of CMOS technologies has greatly benefited the areas of digital design, digital signal processing, and the design of processor architectures, allowing the development and implementation of increasingly complex digital systems and algorithms [1]. Because current digital systems have high switching speeds, the timing resolution of digital circuits has greatly excelled compared to the voltage resolution of analog circuits implemented on CMOS scales of nanometer technologies [2]. This leads to a new approach to signal processing: Time-Mode Signal processing (TMSP).

The arrangement for TI evaluation is shown in Figure 1, where a time instant is measured between the changing edges of two voltage pulses connected to the *Start* and *Stop* inputs of the Time Interval Meter (TIM) [3]. This two pulses can be developed by comparators or discriminators,

which are handled in order to obtain information from signals coming from sensors or detectors of various temporal events, such as radiation flashes in systems using Positron Emission Tomography (PET) [4] and Single Photon Emission Computed Tomography (SPECT) [5]. TIMs execute the count of a time-lapse τ into a binary word. Therefore, a TIM is also called a Time-to-Digital converter (TDC). A TDC is liable for turning a time interval between two clock signals into a digital character.

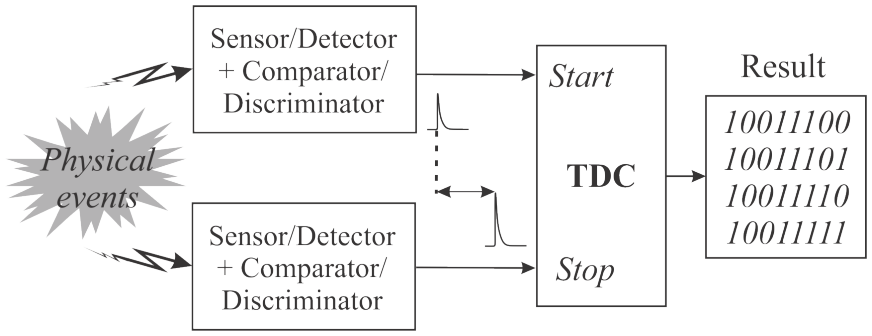

Figure 1. Principle of time-lapse measurement.

In this work, we propose a TDC structure that is composed of two nested counters. The remainder of this paper proceeds as follows. First, Section II describes in detail how the presented structure is composed, as well as a brief description of the operation of its blocks. Then, the experimental results are presented in section III and in the last part, section IV the conclusions of this work are discussed.

Proposed structure

The block diagram of proposed structure is ilustred in Figure 2, which is an 8-bit TDC, the system made up of two nested 4-bit counters, two logic-digital control networks, two registers and a decoder. This proposal has the advantage of having a great integration capacity and high resolution and range. The TDC operating mechanism proposed is as follows. The digital logic blocks are in charge of handling external signals to the converter to obtain the clock signals *CLK* and *CLK1*, for counters 1 and 2 correspondingly.

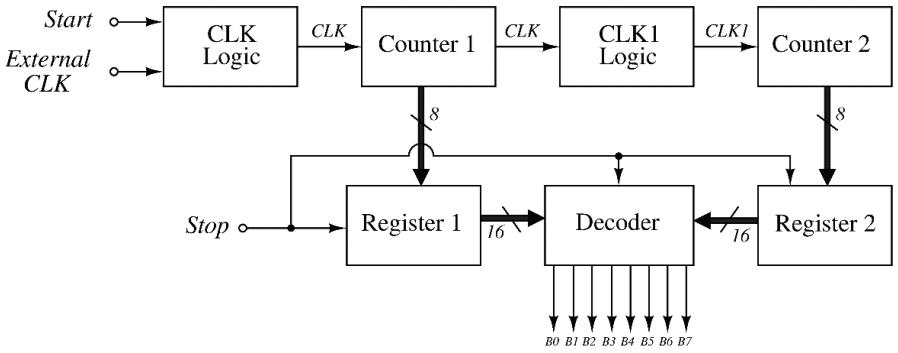

Figure 2. Block diagram of the proposed 8-bit TDC.

The counter blocks are in charge of measuring the time interval between the *Start* and *Stop* pulses. Likewise, the two registers blocks save the state in which the counters stay when the *Stop* pulse occurs. Finally, the binary word stored in each register enters to a decoder that is responsible for delivering a standard 8-bit word to the output of the converter. The implementation

of the counters where based on Johnson type (ring) structure [5], the above is due to the fact that our counter is intended to have a minimum gate delay. Johnson type counters have the characteristic that in each count only one element is activated, that is, there would only be a minimum gate delay between counter events.

The decoder block was proposed under a semi-dynamic logic [6]. The set (1) shows the logic functions used for the 8-bit output of the decoders, where the functions of the bits *B1* to *B4* are obtained by logic values that go from Q_1 to Q_8, which are the outputs corresponding to register 1. Functions of the bits *B5* to *B8* are similar to the previous ones, except that now the values given by register 2 are used. The type of logic used in this work allows decoding with lower power consumption.

$$B1 = Q_8 \cdot \overline{Q_7} + \overline{Q_8} \cdot Q_7 + Q_6 \cdot \overline{Q_5} + \overline{Q_6} \cdot Q_5 + Q_4 \cdot \overline{Q_3} + \overline{Q_4} \cdot Q_3 + Q_2 \cdot \overline{Q_1} + \overline{Q_2} \cdot Q_1 \quad (1a)$$

$$B2 = Q_5 \cdot Q_4 \cdot \overline{Q_7} + \overline{Q_5} \cdot \overline{Q_4} \cdot Q_7 + Q_3 \cdot \overline{Q_1} + \overline{Q_3} \cdot Q_1 \quad (1b)$$

$$B3 = Q_8 \cdot Q_5 \cdot \overline{Q_1} + \overline{Q_8} \cdot \overline{Q_5} \cdot Q_1 \quad (1c)$$

$$B4 = Q_1 \quad (1d)$$

Experimental results

After designing the proposed structure, the layout of the TDC was made using TSMC 180 nm CMOS technology. The developed prototype uses an area of 508 µm x 225 µm and is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a decoder. A microphotography of the TDC that was elaborated can be observed in Figure 3. The circuit has an 8-bits digital output and is powered with a supply of 1.8 V with a total power consumption of 32.4 mW.

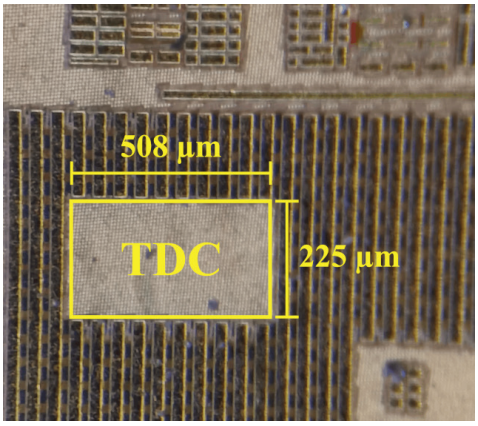

Figure 3. Microphotography of the proposed TDC.

The first test to be performed was to verify the behavior of the system in general; this was done by verifying the performance of the control logic responsible for generating the *CLK* and *CLK1* signals. The test was performed by connecting the device under test to the *Keithley programmable 3-channel DC power supply 2230-30-1*, the power supply voltage for the circuit

is 1.8 V. Additionally, a *WaveStation 3162 Teledyne LeCroy 2-channel Function Generator* was used by selecting a 1.8 V amplitude square wave output with a frequency of 1 MHz and a dutty cycle of 50%, this signal was connected to the *External CLK* input of the system.

In addition to the input signal described above, the *Start* signal of the system was enabled at a fixed value of 1.8 V, this in order to display the signals of interest for this test. The signals were visualized using a *Tektronix Digital Oscilloscope DPO7104*, in the Figure 4 shows the results of this test. The *CLK1* signal is produced every 16 events of the *CLK* signal, which serves to control the events of the two counters. Corroborating the function of these two signals we can make sure that the innards of the system is working properly.

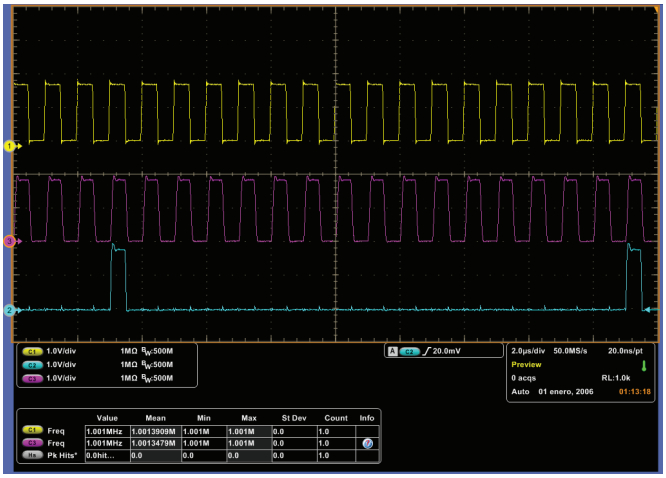

Figure 4. External clock signal and internal clock signals CKL and CLK1 of the proposed TDC.

The next test performed to the proposed TDC is to obtain all the count codes for the 8-bit output. To perform this measurement, two out of phase clock signals were used for the *External CLK* and *Start* inputs, the frequency, amplitude and dutty cycle of the signals is the same as in the previous test. To obtain the results of this test, a *Keysight 16851A 34-Channel Logic Analyzer* was used, which were configured to get the logic states of the output bus and the signals of interest to be measured.

The results of this measurement are presented in Figure 5, where part of the output codes obtained can be observed, being these from code 114 to 120. Subsequently, in Figure 6 a graph with the characteristic curve is observed, which contains all the output codes for the complete conversion range of the TDC, it should be noted that an approach to the graph was made in the same interval as the capture made to the logic analyzer.

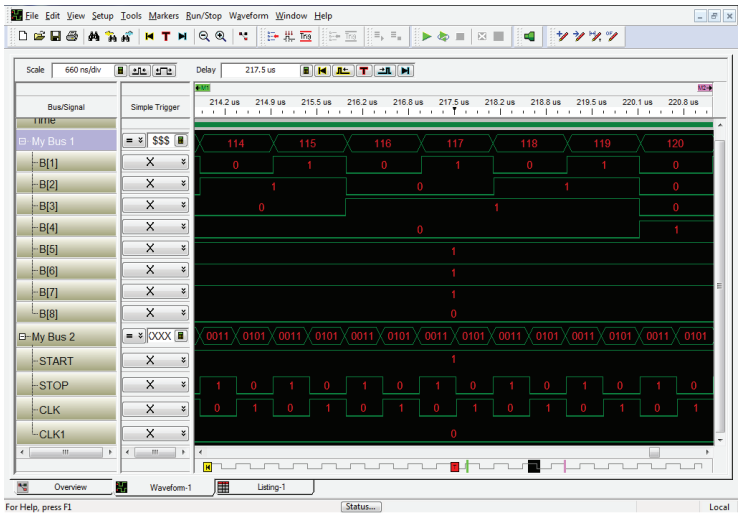

Figure 5. Screenshot of the TDC characteristic curve measurement.

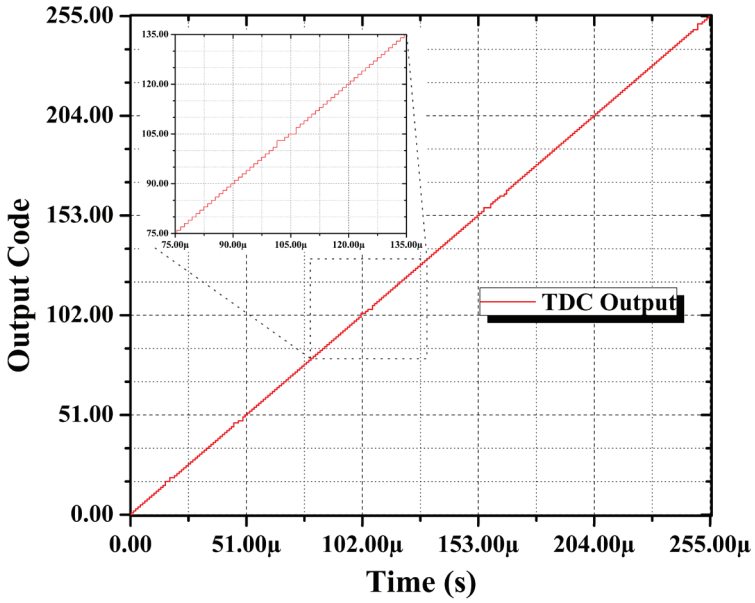

Figure 6. Characteristic curve of the proposed TDC.

Finally, a single-shot test was performed by configuring the TDC input time interval to keep it fixed during the measurement; the purpose of this is to obtain the standard deviation (σ) of the output distribution. The test was performed by taking 1000 samples of a fixed conversion interval with an output code of 117. The results of the single-shot test are shown in Figure 7, the standard deviation obtained was 0.78 LSB for this input conversion interval.

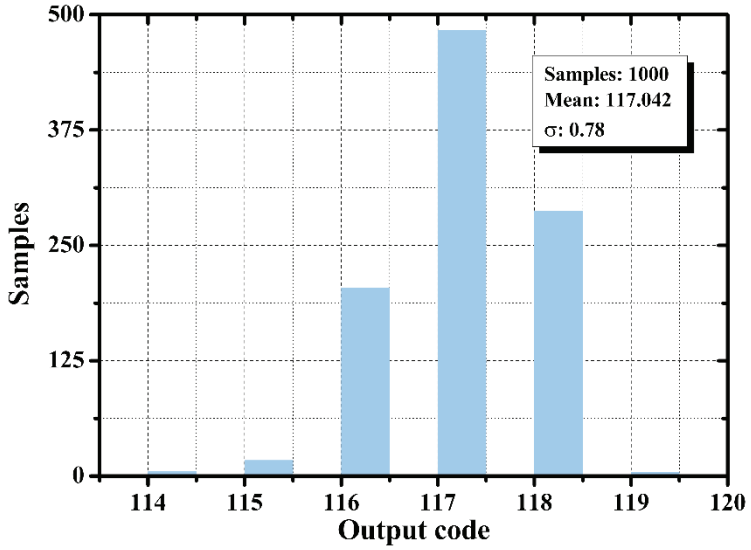

Figure 7. Test result the single-shot code distribution of the proposed TDC.

The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC, the tests performed affirm that it is possible to develop simple structures with outstanding performance using mature 180 nm technology.

Summary and conclusions

One of the many favorable consequences of technological scaling is that the time resolution of digital circuits has surpassed the voltage resolution of its analog counterpart. TDC's are widely used system to perform time-mode processing because they are easy to implement due to their simple structures and the diverse variety of applications they have. Along with the structure presented hereunder we intend not pursue an ordinary delay line configuration. With this configuration that makes use of two nested counters, good repeatability results can be obtained and although in certain cases output code errors do occur, these can be minimized by using layout techniques such as the implementation of ground planes, as well as increasing the operating frequency by using special high-speed output pads, thus improving the time resolution which is a very important feature of TDS's.

Time-mode signal processing arises as a response to the need to study new physical phenomena that occur with such small magnitudes and at such high speeds that were previously considered non-existent. Therefore, the study of time-to-digital converters offers a wide area of opportunity for the development of various fields of research and technological advances in the future.

Acknowledgment

The authors would like to thank the National Council of Science and Technology, Mexico (CONACyT) for the for the doctoral grant A1-S-43214. We also thank the National Institute of Astrophysics, Optics and Electronics (INAOE) for the technical training and for providing the use of their laboratories and equipment. And last but not least, we thank the R9 EDS ASIC Design Fabrication contest organizing and judging committee for choosing our design as the winner.

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An 8-bit TDC implemented with two nested Johnson counters

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I. Introduction

THE channel length reduction and node scalling of CMOS technologies has greatly benefited the areas of digital design, digital signal processing, and the design of processor architectures, allowing the development and implementation of increasingly complex digital systems and algorithms. The arrangement for TI evaluation is shown in Fig. 1, where a time instant is measured between the changing edges of two voltage pulses connected to the *Start* and *Stop* inputs of the Time Interval Meter (TIM). TIMs execute the count of a time-lapse τ into a binary word. Therefore, a TIM is also called a Time-to-Digital converter (TDC). A TDC is liable for turning a time interval between two clock signals into a digital character.

In this work we propose a TDC structure which is composed of two nested counters. The remainder of this paper proceeds as follows. First, section II describes in detail how the presented structure is composed, as well as a brief description of the operation of its blocks. Then, the experimental results are presented in section III and in the last part, section IV the conclusions of this work are discussed.

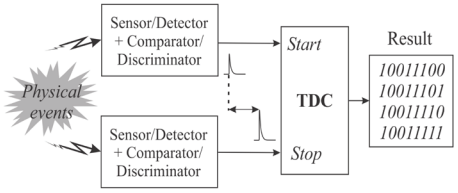

Fig. 1. Principle of time-lapse measurement.

II. Proposed Structure

The block diagram of proposed structure is ilustred in Fig. 2, which is an 8-bit TDC, the system made up of two nested 4-bit counters, two logic-digital control networks, two registers and a decoder. The digital logic blocks are in charge of handling external signals to the converter to obtain the clock signals *CLK* and *CLK1*, for counters 1 and 2 correspondingly.

The implementation of the counters where based on Johnson type (ring) structure, the above is due to the fact that our counter is intended to have a minimum gate delay. The decoder block was proposed under a semi-dynamic logic. The type of logic used in this work allows decoding with lower power consumption.

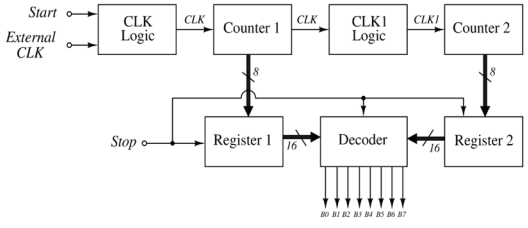

Fig. 2. Block diagram of the proposed 8-bit TDC.

III. Experimental Results

After designing the proposed structure, the layout of the TDC was made using TSMC 180 *nm* CMOS technology. The developed prototype uses an area of 508 *µm* x 225 *µm* and is composed of two 4-bit nested counters, two digital-logic control networks, two registers and a decoder. A microphotography of the TDC that was elaborated can be observed in Fig. 3. The circuit has an 8-bits digital output and is powered with a supply of 1.8 *V* with a total power consumption of 32.4 *mW*.

The next test performed to the proposed TDC is to obtain all the count codes for the 8-bit output. The results of this measurement are presented in Fig. 4, in which a graph with the characteristic curve is observed, which contains all the output codes for the complete conversion range of the TDC.

Finally, a single-shot test was performed by configuring the TDC input time interval to keep it fixed during the measurement, the purpose of this is to obtain the standard deviation σ of the output distribution. The results of the single-shot test are shown in Fig. 5, the standard deviation obtained was 0.78 *LSB* for this input conversion interval.

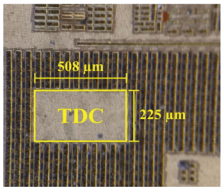

Fig. 3. Microphotography of the proposed TDC.

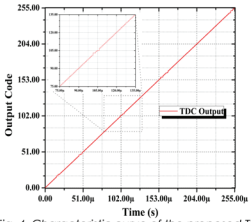

Fig. 4. Characteristic curve of the proposed TDC.

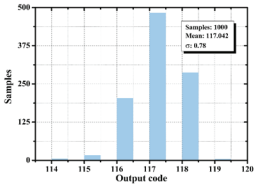

Fig. 5. Test result the single-shot code distribution of the proposed TDC.

IV. Conclusions

The proposed structure shows good performance results and repeatability for continuous conversion conditions, these results are attributed to the simplicity of the system and the use of counters with minimum gate delay as the main elements for the TDC, the tests performed affirm that it is possible to develop simple structures with outstanding performance using mature 0.18 µm technology.

Time-mode signal processing arises as a response to the need to study new physical phenomena that occur with such small magnitudes and at such high speeds that were previously considered non-existent. Therefore, the study of time-to-digital converters offers a wide area of opportunity for the development of various fields of research and technological advances in the future.

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Illustration 1. Presented Poster at LAEDC 2022.

A Single Memristor-based TTL NOT logic

Una única lógica NOT TTL basada en Memristor

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Keywords

Memristor; NOT logic; TTL; hysteresis; green electronics; biodegradable electronics.

Abstract

This article presents a NOT logic gate circuit based on a single memristor, and analyzes it for different biological memristive samples based on extracted resistances. The simple resistor-voltage representation of the memristor in the logic circuit is used to formulate a methodology to tune the parameters of the circuit in accordance with TTL voltage values. The logic circuit consists of two resistors in series with the memristor. The input is connected to one end of the memristor, and the output is drawn across the series connection of the second resistor, and the memristor. The methodology comprises of two steps, where, in the first step, the logic 'low' TTL-input voltages are examined, and in the second step, the circuit is evaluated for logic 'high' TTL-input voltages. The methodology reveals that there is a mínimum voltage value of 'high' TTL-input beyond which the output does not fall within the logic 'low' TTL-output. The proposed technique may be extended to evaluate novel memristive materials for single memristor-based NOT logic.

Palabras clave

memristor; NO lógica; TTL; histéresis; electrónica verde; electrónica biodegradable.

Resumen

Este artículo presenta un circuito de puerta NO lógica basado en un solo memristor y lo analiza para diferentes muestras biológicas memristivas basadas en resistencias extraídas. La representación simple de voltaje de resistencia del memristor en el circuito lógico se usa para formular una metodología para ajustar los parámetros del circuito de acuerdo con los valores de voltaje TTL. El circuito lógico consta de dos resistencias en serie con el memristor. La entrada está conectada a un extremo del memristor y la salida se dibuja a través de la conexión en serie de la segunda resistencia y el memristor. La metodología consta de dos pasos, donde, en el primer paso, se examinan los voltajes de entrada TTL "bajos" lógicos, y en el segundo paso, se evalúa el circuito para voltajes de entrada TTL "altos" lógicos. La metodología revela que hay un valor de voltaje mínimo de entrada TTL "alta" más allá del cual la salida no cae dentro de la salida TTL lógica "baja". La técnica propuesta puede extenderse para evaluar nuevos materiales memristivos para la lógica NOT basada en un solo memristor.

Introduction

Leon Chua's proposal of the fourth passive element, the memristor, relates flux, and charge [1]. Since the inception of the TiO2 based memristor in 2008, the possibilities of exploration of memristors, and their applications have increased [2]. To realize such applications, the implementation of memristor-based digital logic circuits in TTL/ CMOS compatible style has always been essential. As of now, IMPLY, and MAGIC style of logic designs have been proposed, which, as opposed to TTL/ CMOS-based operation, are sequential in nature [3][4]. Memristive action has also been reported in biological materials like sweat ducts, Venus flytrap plant, and amoeba [1]. Biomaterial-based memristors have the potential to contribute to next-generation flexible, and green electronics.

This article proposes the concept of a NOT logic gate using a resistor-bias model of a single memristor compatible with TTL mode of operation. The logic based on TTL votages is applied to a number of reported biological memristors which give pinched hysterics loop in V-I plane. The

high off-state resistance, R_H, and low on-state resistance, R_L, are extracted from V-I plots of the reported samples. A simple methodology is proposed for setting up the circuit parameters, and voltage range of operation as per TTL.

Methodology

The proposed memristor-based NOT logic circuit is shown in Fig. 1 (a). The circuit consists of two resistors, R_1 and R_2 , connected in series with the memristor. The memristor resistance is represented as R_M. The input voltage, V_{IN}, corresponding to logic '0' or logic '1' is applied to one terminal of the memristor, and the other terminal is connected to the resistor, R_2. The output voltage, V_{OUT}, is taken across the series connection of R_2, and R_M as depicted in Fig. 1 (a). Depending on the input, R_M changes. If V_{IN} = '1', $R_M = R_L$, and if V_{IN} = '0', $R_M = R_H$, where, R_H, and R_L are high, and low resistances in off-state, and on-state respectively.

The methodology for tuning the circuit parameters as carried out on LTspice XVII is shown in Fig. 1 (b). The output voltage is given by $V_{OUT} = {(V_{CC} - V_{IN})(R_2 + R_M)}\Big/{(R_1 + R_2 + R_M)}$. If $m = \frac{R_1}{R_2 + R_M}$, such that $R_1 = R_2$, we arrive at the relationship $R_1 = R_2 = \frac{m}{1-m} R_M$.

Results

Step I

For 10 biological memristors from literature as listed in Table I, taking m = 0.01, R_1, and R_2 are calculated, and considered in the circuit where a sweep of V_{IN} is done from 0 V – 0.8 V, having $R_M = R_H$, and V_{OUT} is plotted in Fig. 1 (c). It is observed that the values lie well within the TTL logic '1' range of 2 V – 5 V, and closer to 5 V for the range of TTL V_{IN}. The plots for all samples are exactly same because considering the conditions, we arrive at $V_{OUT} = V_H = \frac{(V_{CC} - V_L)(n+1)}{(2n+1)}$, where $n = \frac{m}{1-m}$ is a constant.

Step II

Carrying forward R_1, and R_2 as obtained from the previous step, a sweep of V_{IN} is done from 2 V – 5 V, having $R_M = R_L$, and V_{OUT} is plotted in Fig. 2 (a). In this case, $V_{OUT} = V_L = \frac{(V_{CC} - V_H)(nr+1)}{(2nr+1)}$, where, $r = {R_H}\Big/{R_L}$. Since R_1, and R_2 are dependent on R_H, therefore, some values of V_{OUT} may lie outside the TTL logic '0' voltages corresponding to 0 V – 0.8 V. This further indicates that there is supposed to be a minimum value of $V_{IN} = V_{H,min}$ for which $V_{OUT} = V_L$ lies in the TTL logic '0' range. This is indicated by a shaded region in Fig. 2 (a), and listed in Table I.

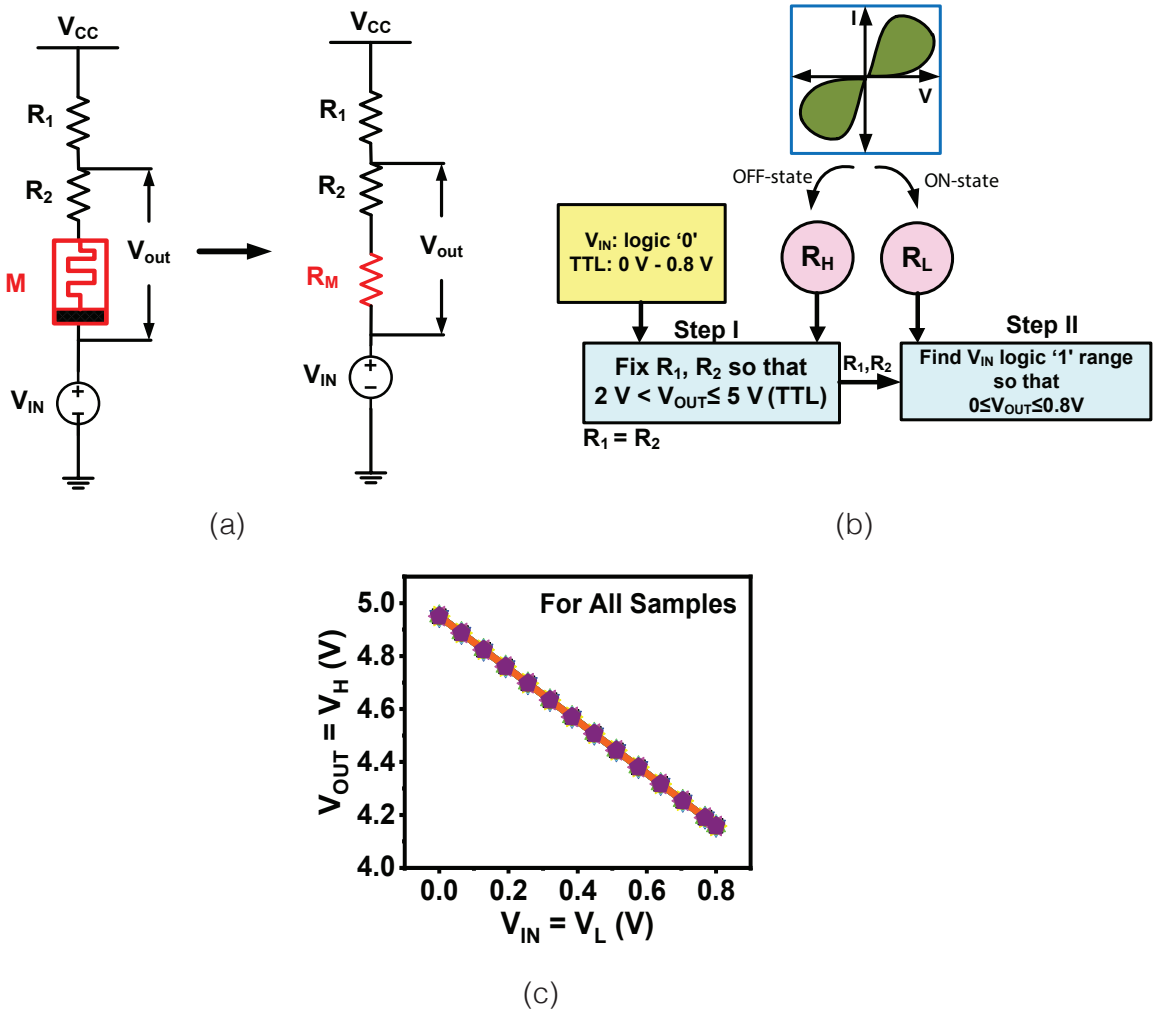

Figure 1. (a) NOT logic circuit using memristor polarity; (b) Flowchart showing the methodology; (c) $V_{OUT} = V_H$ versus $V_{IN} = V_L$ plot

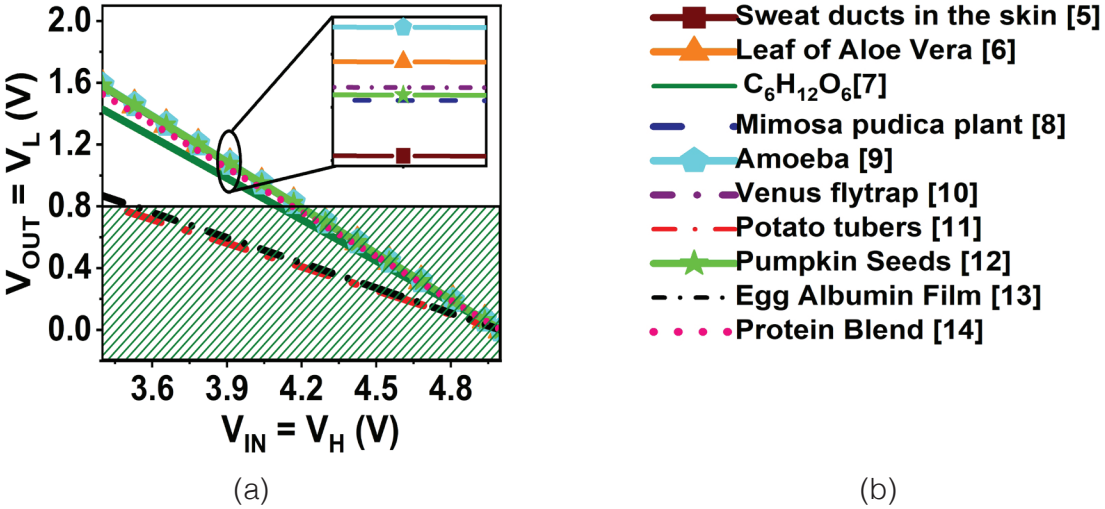

Figure 2. (a) $V_{OUT} = V_L$ versus $V_{IN} = V_H$ plot showing the valid TTL $V_{OUT} = V_L$ limit; (b) Legend for (a)

Table 1. Table for TTL Logic Showing R_H, R_L, r, R_1, R_2, $V_{H,min}$

Sl. No.	Memristor TTL NOT Logic Parameters				
	$R_H(k\Omega)$	$R_L(k\Omega)$	$r = R_H/R_L$	$R_1 = R_2$	$V_{IN} = V_{H,min}(V)$
[5]	417	360	1.15	4.21 kΩ	4.19
[6]	321	218	1.47	3.24kΩ	4.18
[7]	1.96	0.14516	13.5	19.79 Ω	4.10
[8]	108	88	1.22	1.09 kΩ	4.19
[9]	16	14	1.14	161Ω	4.19
[10]	73	69	1.05	737.3Ω	4.19
[11]	6060	2042	2.98	61.5kΩ	4.17
[12]	419	393	1.06	4.2kΩ	4.19
[13]	31.8	0.06	530	321Ω	3.52
[14]	1.112	0.4	2.78	11.23Ω	4.17

Conclusions

This work presented a simple circuit to implement a NOT logic gate by using a single memristor, and differential output. Considering 10 biological sample from literature, the conclusions of this article can be summed up as follows.

- The fixed resistors in the circuit, R_1 and R_2, which are equal, and proportional to R_H, were fixed by taking a value of m for logic '0' TTL input. In this article, m = 0.01 was considered.
- The resistors, R_1 and R_2, once fixed, were considered for logic '1' TTL input corresponding to which, the entire logic '0' TTL output was achieved for all samples.
- The same approach may be used for CMOS logic.

Acknowledgement

The authors specially acknowledge article [1] by L. Chua as a reference material for the work.

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A Single Memristor-Based TTL NOT Logic

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Introduction

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This article proposes the concept of a NOT logic gate using a resistor-bias model of a single memristor compatible with TTL mode of operation. The logic based on TTL voltages is applied to a number of reported biological memristors which give pinched hysterics loop in V-I plane. The high off-state resistance, R_H, and low on-state resistance, R_L, are extracted from V-I plots of the reported samples. A simple methodology is proposed for setting up the circuit parameters, and voltage range of operation as per TTL.

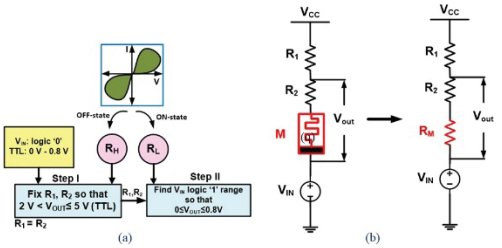

Fig. 1 (a) Flowchart showing the methodology; **(b)** NOT logic circuit using memristor polarity; **(c)** $V_{OUT} = V_H$ versus $V_{IN} = V_L$ plot

Results and Discussion

Step I: For 10 biological memristors from literature as listed in Table I, taking $m = 0.01$, R_1, and R_2 are calculated, and considered in the circuit where a sweep of V_{IN} is done from 0 V – 0.8 V, having $R_M = R_H$, and V_{OUT} is plotted in Fig. 1 (c). It is observed that the values lie well within the TTL logic '1' range of 2 V – 5 V, and closer to 5 V for the range of TTL V_{IN}. The plots for all samples are exactly same because considering the conditions, we arrive at $V_{OUT} = V_H = \frac{(V_{CC}-V_L)(n+1)}{(2n+1)}$, where $n = \frac{m}{1-m}$ is a constant.

Step II: Carrying forward R_1, and R_2 as obtained from the previous step, a sweep of V_{IN} is done from 2 V – 5 V, having $R_M = R_L$, and V_{OUT} is plotted in Fig. 2 (a). In this case, $V_{OUT} = V_L = \frac{(V_{CC}-V_H)(nr+1)}{(2nr+1)}$, where, $r = {}^{R_H}/_{R_L}$. Since R_1, and R_2 are dependent on R_H, therefore, some values of V_{OUT} may lie outside the TTL logic '0' voltages corresponding to 0 V – 0.8 V. This further indicates that there is supposed to be a minimum value of $V_{IN} = V_{H,min}$ for which $V_{OUT} = V_L$ lies in the TTL logic '0' range. This is indicated by a shaded region in Fig. 2 (a), and listed in Table I.

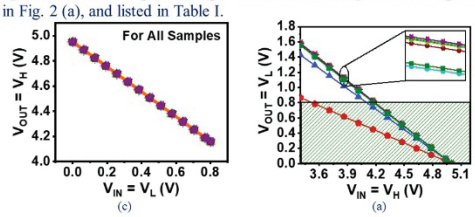

Fig. 2 (a) $V_{OUT} = V_L$ versus $V_{IN} = V_H$ plot showing the valid TTL $V_{OUT} = V_L$ limit

TABLE I: TABLE FOR TTL LOGIC SHOWING $R_H, R_L, r, R_1, R_2, V_{H,min}$

Sl. No.	Sample	Memristor TTL NOT Logic Parameters				
		$R_H(k\Omega)$	$R_L(k\Omega)$	$r = {}^{R_H}/_{R_L}$	$R_1 = R_2$	$V_{IN} = V_{H,min}(V)$
1	Sweat ducts	417	360	1.15	4.21 kΩ	4.19
2	Aloe Vera	321	218	1.47	3.24kΩ	4.18
3	Glucose	1.96	0.14516	13.5	19.79 Ω	4.10
4	Mimosa Pudica	108	88	1.22	1.09 kΩ	4.19
5	Amoeba	16	14	1.14	161Ω	4.19
6	Venus flytrap	73	69	1.05	737.3Ω	4.19
7	Potato tubers	6060	2042	2.98	61.5kΩ	4.17
8	Pumpkin Seeds	419	393	1.06	4.2kΩ	4.19
9	Egg albumin	31.8	0.06	530	321Ω	3.52
10	Protein blend	1.112	0.4	2.78	11.23Ω	4.17

Materials and Methods

The methodology for tuning the circuit parameters as carried out on LTspice XVII is shown in Fig. 1 (b). The output voltage is given by $V_{OUT} = {}^{(V_{CC}-V_{IN})(R_2+R_M)}/_{(R_1+R_2+R_M)}$. If $m = \frac{R_1}{R_2+R_M}$, such that $R_1 = R_2$, we arrive at the relationship $R_1 = R_2 = \frac{m}{1-m}R_M$.

Conclusions / Next Steps

This work presented a simple circuit to implement a NOT logic gate by using a single memristor, and differential output. Considering 10 biological sample from literature, the conclusions of this article can be summed up as follows.

- The fixed resistors in the circuit, R_1, and R_2, which are equal, and proportional to R_H, were fixed by taking a value of m for logic '0' TTL input. In this article, $m = 0.01$ was considered.
- The resistors, R_1, and R_2, once fixed, were considered for logic '1' TTL input corresponding to which, the entire logic '0' TTL output was achieved for all samples.
- The same approach may be used for CMOS logic.

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Illustration 1. Presented poster at LAEDC 2022.