Comparative study of steep switching devices for 1T dynamic memory

Estudio comparativo de dispositivos de conmutación rápida para memoria dinámica 1T

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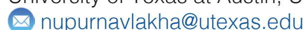
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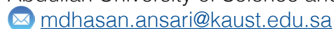
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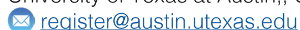
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Keywords

Dynamic memory; capacitorless; tunnel field effect transistor; zero sub-threshold swing; zero impact ionization FET; thin-capacitively coupled thyristor; field effect diode; retention time; power.

Abstract

This work focuses on understanding the operation and performance of various steep switching devices (subthreshold slope sub 60 mV/decade), namely Thin-Capacitively Coupled Thyristor (TCCT), Field Effect Diode (FED), Zero sub-threshold swing and Zero impact ionization FET (Z^2-FET), and Tunnel Field Effect Transistor (TFET) as capacitorless dynamic memory. Functionality as 1T DRAM depends on creation of potential well which must be induced in a p-i-n structure, achieved through precise doping of p-region (TCCT), asymmetric gate alignment (Z^2FET, TFET) and use of two independent gates (FED and twin gate TFET). While TCCT, FED and Z^2FET operate in forward bias, TFET operates in reverse bias. The work shows a comparative analysis of these devices in terms of retention time, sense margin, current ratio, power and speed which are crucial metrics for future DRAMs and also provides a guideline for application specific design.

Palabras clave

Memoria dinámica, sin condensador, transistor de efecto de campo de túnel, oscilación de subumbral cero; FET de ionización de impacto cero, tiristor de acoplamiento capacitivo delgado, diodo de efecto de campo, tiempo de retención, potencia.

Resumen

Este trabajo se centra en entender la operación y el rendimiento de varios dispositivos de conmutación abrupta (pendiente subumbral inferior a 60 mV/década), a saber, el Tiristor de Acoplamiento Capacitivo Delgado (TCCT, por sus siglas en inglés), el Diodo de Efecto de Campo (FED), el FET de Pendiente Subumbral Cero y Cero Ionización de Impacto (Z^2-FET) y el Transistor de Efecto de Túnel (TFET) como memoria dinámica sin condensador. La funcionalidad como 1T DRAM depende de la creación de un pozo de potencial que debe ser inducido en una estructura p-i-n, lo cual se logra mediante el dopaje preciso de la región p (TCCT), la alineación asimétrica de la compuerta (Z^2FET, TFET) y el uso de dos compuertas independientes (FED y TFET de doble compuerta). Mientras que el TCCT, el FED y el Z2FET operan en polarización directa, el TFET opera en polarización inversa. El trabajo muestra un análisis comparativo de estos dispositivos en términos de tiempo de retención, margen de detección, relación de corriente, potencia y velocidad, que son métricas cruciales para las futuras DRAMs, y también proporciona una guía para el diseño específico de aplicaciones.

Introduction

In the conventional DRAM cell (1T-1C), data is stored in the capacitor as electrical charge that leaks over time. Scaling the capacitor is the most critical issue in DRAM as it reduces the charge storage [1-3]. This adversely affects the charge retention, and thus, requires more refresh cycles [1]. Moreover, transistor scaling leads to higher leakage current that results in higher power dissipation and reduction in retention time. Thus, high retention is essential to reduce refresh cycles that consume ~40-50% of energy in off-chip memory hierarchy [1]. Due to difficulty in scaling the capacitor associated with the conventional DRAM cell [1-3], the single transistor (1T)

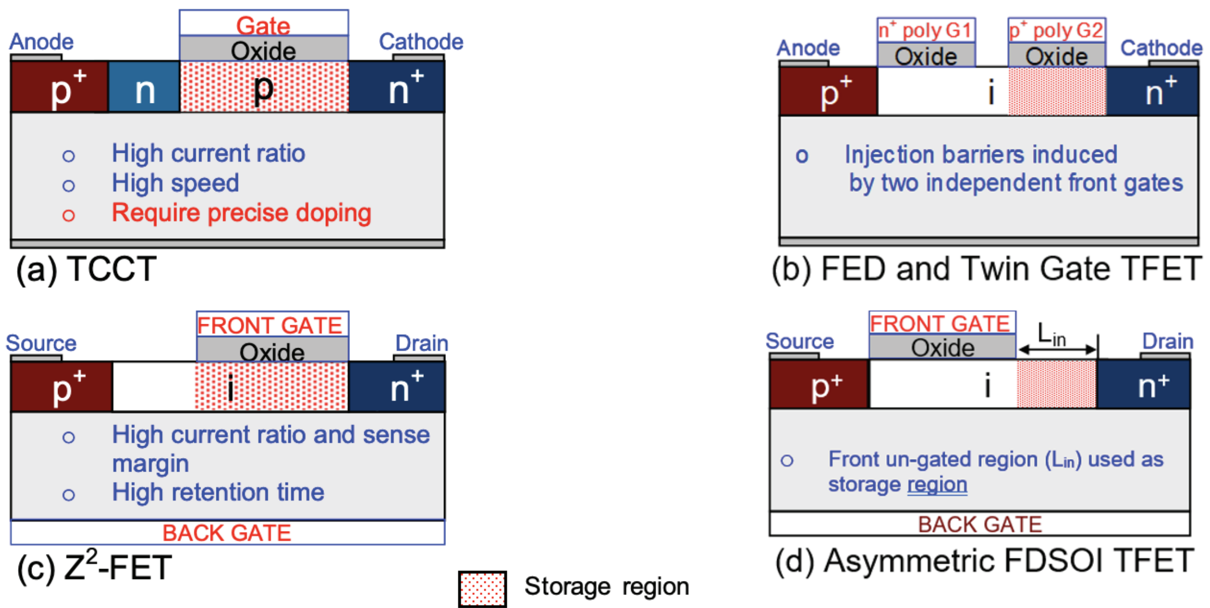
cells [2] have been proposed. Further, the quest for DRAM with high retention and low power necessitates use of steep switching devices as dynamic memory [3-9]. These devices are p-i-n FETs (have different types of dopants for source and drain) and include Thin-Capacitively Coupled Thyristor (TCCT) [3,4], Field Effect Diode (FED) [5], Zero sub-threshold swing and Zero impact ionization FET (Z^2-FET) [6,7], and Tunnel Field Effect Transistor (TFET) [8,9].

Device Operation

TCCT, FED and Z^2-FET (Figs. 1(a)-(c)) exhibits a very steep transition from off-to-on state, operate in forward bias and utilize the positive feedback mechanism for conduction while TFET (Fig. 1(d)) operates in reverse bias and utilize band-to-band tunneling mechanism for conduction. These devices form a *p-n-p-n* structure with an electron (V_n) and hole (V_p) injection barriers (Fig. 1(e)). When electrons are injected into the channel, a few of the holes accumulated in the barrier reduce the barrier height for electrons and so does the electron accumulation for conduction due to holes [5,6]. The charge reposition increases the conduction that further reduces the barrier heights, and thus, a feedback mechanism is triggered.

Device as 1T Dynamic Memory

An essential requirement for all types of dynamic memories is the storage area for charge carriers. In *n*MOSFETs, *p*-type body implicitly behaves as the storage region (Fig. 2 (a)) [4], however for the devices with a p^+-i-n^+ structure, the creation of potential well is critical as electrostatic potential well is not implicitly formed, as shown in Fig. 2(b). Therefore, the architecture is modified to be used as capacitorless DRAM.



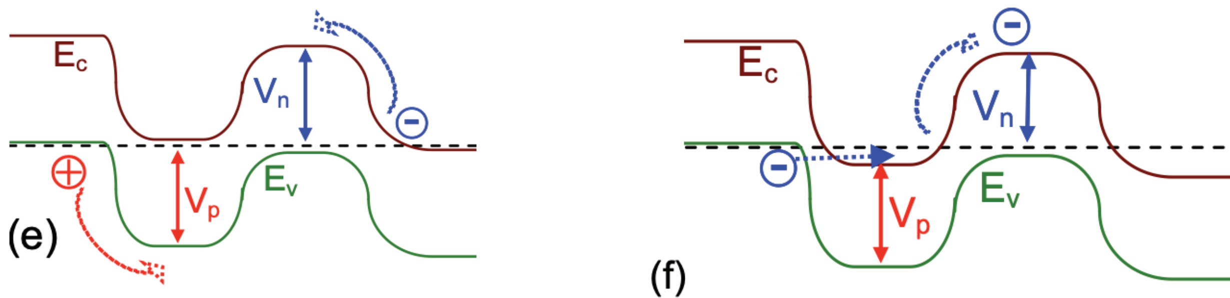


Figure 1. Schematic diagram of (a) TCCT, (b) FED and Twin gate TFET, (c) Z²-FET, and (d) asymmetric TFET along with their storage region, represented by shaded region. (e) Operating mechanism for TCCT, FED, Z²-FET, and (f) for TFET demonstrated through energy band diagrams. V_n and V_p are the electron and hole injection barriers, respectively.

In thyristor-based feedback action [3], the injection barriers are formed through precise doping of *p*-type and *n*-type regions in the channel (Fig. 1(a)). This triggers a doping dependent bipolar action. The device utilizes the *p*-type doped region in the channel for charge storage. FED [5] utilizes two independent front gates with different gate workfunction (n^+ poly ~ 4.25 eV and p^+ poly ~ 5.2 eV) to create different injection barriers (Fig. 1(b)). Similar structure is used as twin gate TFET [9] with region under p^+ poly gate as storage region. Z²-FET (Fig. 1(c)) exploits the region under front gate [7], near n^+ doped drain region for charge storage with back gate biased positively and front gate negatively to create a *p-n-p-n* structure. A similar asymmetric Double Gate TFET in Fig. 1(d) is utilized as DRAM [8]. Unlike Z²-FET, TFET operates in reverse bias in the read operation and utilizes the underlap region for charge storage.

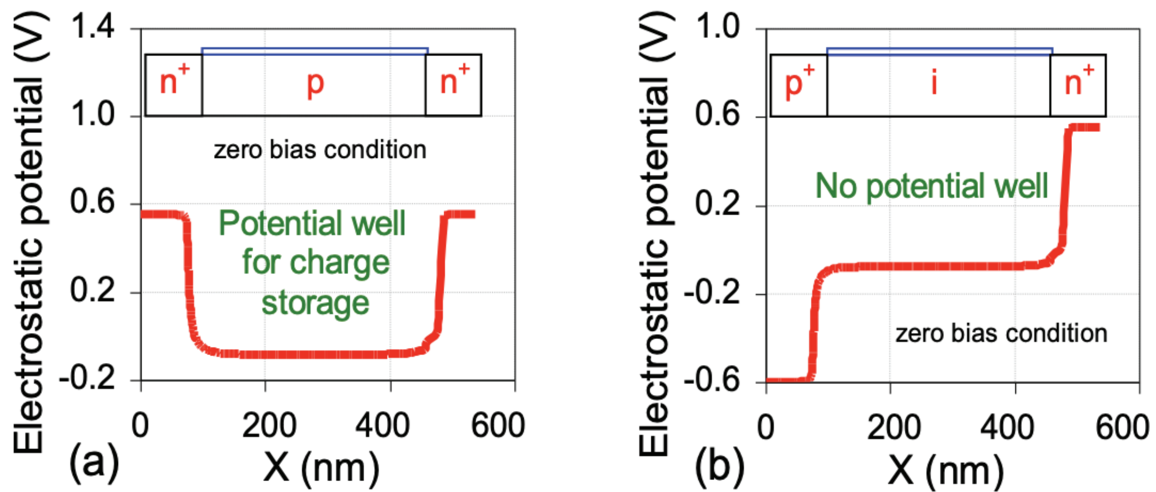


Figure 2. Variation in electrostatic potential along the channel direction (X) for (a) conventional *n-type* MOS and (b) TFET.

DRAM operation is based on generation and recombination of holes in the storage region. Storage of the majority excess carriers (holes) is defined as write '1' and the removal is termed as write '0' [4]. Fig. 3 illustrates DRAM operation and defines the performance metrics. Q_{INIT} indicates the charge in the storage region at zero bias, the charge stored between state '1' and state '0' is during write operation ($\Delta Q_W = Q_{W1} - Q_{W0}$) which decays during hold operation ($\Delta Q_H = Q_{H1} - Q_{H0;}\ \Delta Q_W > \Delta Q_H$) due to hole recombination ($-\Delta Q_{hh1}$) for state '1' and hole generation ($+\Delta Q_{hh0}$) for state '0'. The maintenance of charges (Q_{H1} and Q_{H0}) during hold determine the retention time. Further during read, the hole concentration decreases for state '1' due to diffusion and thermal recombination and the charge difference observable during read ($\Delta Q_R = Q_{R1} - Q_{R0};$) determine the sense margin.

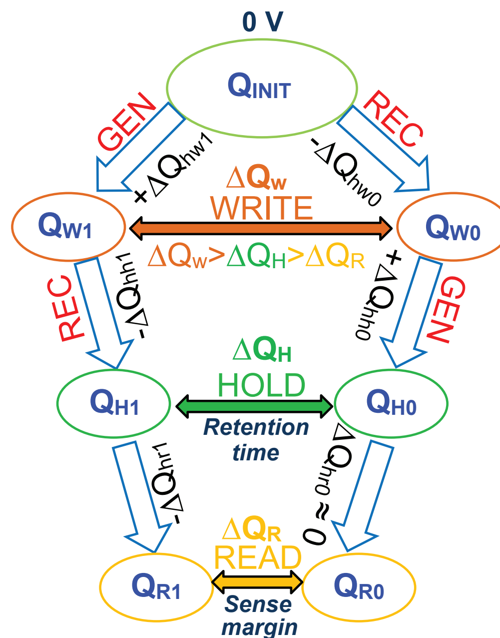


Figure 3. Schematic of charge distribution in potential well for write, hold and read, consecutively.

The power consumed is determined by the voltage applied and current generated during write as shown in Table I, while the speed is evaluated through write time. As observed through the data of Z^{2}FET [8,9] in Table I, power and speed are trade-off. Table shows TFET as most efficient for low power, however the ratio of read currents that determine the current sensitivity is low. TCCT show a high speed but FED memory cell is more flexible than the TCCT cell, and it needs precise control of the film doping profile [5]. Also, nearly intrinsic film has a higher carrier lifetime and thus other p-i-n architectures show a higher retention time (RT) as shown in Fig. 4.

Table 1. Comparison of write time and power during write '1', and current ratio of read currents for state '1' and '0' (I_1/I_0) for different architectures.

Device	L_s (nm)	$\|V_d\|$ (V)	I_d (µA)	Power (µW)	Write time (ns)	Current ratio (I_1/I_0)
TCCT [3]	250	1.2	-	-	2	10^7
TCCT [4]	100	1.2	~15	18	2	10^7
FED [5]	400	1.2	~10^2	120	4	10^7
Z^2-FET [6]	400	1.3	500	650	1	10^7
Z^2-FET [7]	200	0.5	10	5	350	-
TFET [8]	400	0.5	10^{-2}	0.005	~10^3	1
TFET [9]	100	1.0	0.3	0.3	5	10^3

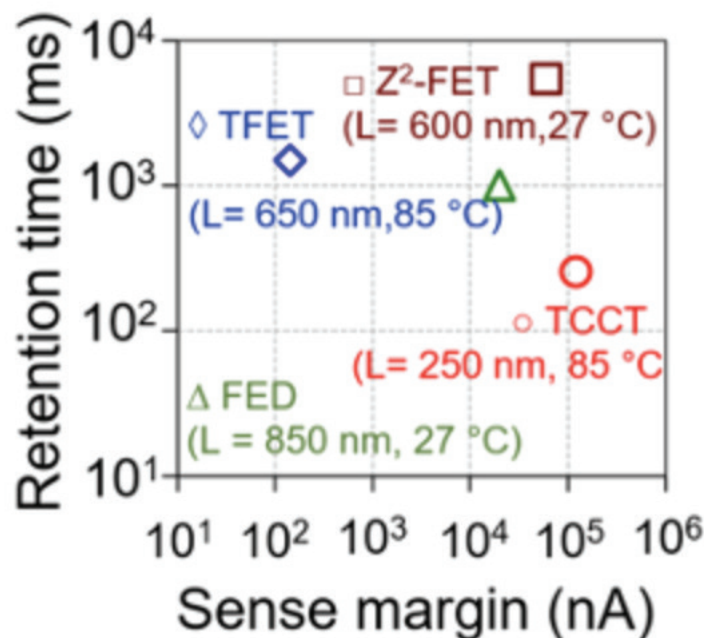


Figure 4. Comparison of retention time and sense margin of various p^+-i-n^+ based architectures (TCCT [3], FED [5], Z^2-FET [7], TFET [9])

Comparing all the structures as in Fig. 4 shows TCCT has a high sense margin (SM) and a good retention characteristic with RT > 100ms at 85 °C, TFET has high RT but a low SM, FED and Z^{2}FET show an optimal performance in terms of both high SM and RT, but Z^{2}FET have shown better and promising results. The study reflects the feasibility of steep devices for low power DRAM and criteria to select among the proposed devices for application specific design.

Conclusion

Steep switching devices have been showing immense potential for replacing conventional MOS transistor as 1T DRAM. Z^2-FET, FED and TCCT based dynamic memories have shown high operating current, current sensing margin and operates in forward bias and utilizes feedback mechanism. TCCT shows fast operation, however, the need of precise doping for storage is a drawback. TFET performance in terms of retention time and power is well-suited, however low sense margin and current ratio is an issue. FED has shown potential as 1T DRAM but Z^2FET have shown promising results. The study reflects the possibility to improve the performance metrics of the proposed devices.

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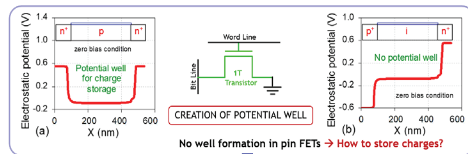
Introduction

Quest for Low Power Capacitorless (1 Transistor) DRAM:

- Capacitor scaling in Conventional DRAMs with 1T – 1C difficult [1]
- Require more refresh cycles and hence, power consumption
- Steep switching devices as Capacitorless DRAM with p⁺ - i -n⁺ structure namely,
  - Thin-Capacitively Coupled Thyristor (TCCT) [2]
  - Field Effect Diode (FED) [3]
  - Zero sub-threshold swing and Zero impact ionization FET (Z^2-FET) [4,5]
  - Tunnel Field Effect Transistor (TFET) [6,7]

Functionality as 1T DRAM



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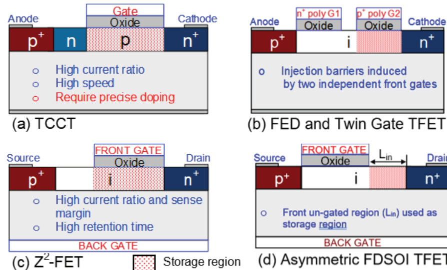
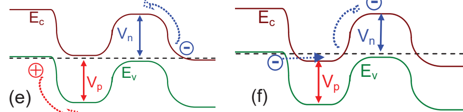
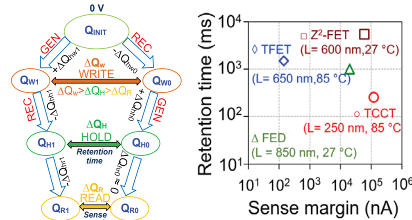




Structure	Storage Region	Mechanism
TCCT	doped p-type region	Forward bias feedback
FED / TFET	p⁺ poly front gate	Forward bias feedback
Z^2FET	Under front gate	Forward bias feedback
Asymmetric TFET	Underlap region	Reverse bias

Results and Discussion

OPERATION & DRAM METRICS



- **TCCT** has a high sense margin (SM) and a good retention characteristic with RT > 100ms at 85 °C
- **TFET** has high RT but a low SM
- **FED and Z^2FET** show an optimal performance in terms of both high SM and RT

Comparison of write time and power during write '1', and current ratio of read currents for state '1' and '0' (I_1/I_0) for different architectures.

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Z^2-FET [6]	200	0.5	10	5	350	-
TFET [7]	400	0.5	10^{-2}	0.005	~10^3	1
TFET [8]	100	1.0	0.3	0.3	5	10^3

Conclusions / Next Steps

- Steep switching devices have potential for replacing conventional MOS transistor for low power applications.
- **Z^2-FET, FED and TCCT** DRAMs have shown high operating current and current sensing margin.
- **TCCT** shows fast operation, however, the need of precise doping for storage is a drawback.
- **TFET** performance in terms of retention time and power is well-suited, however low sense margin and current ratio is an issue.
- **FED** has shown potential as 1T DRAM but lacks extensive study.
- **Z^2FET** have shown promising results amongst all the pin FETs based DRAM.
- Study shows the shortcomings and advantages of each device, reflecting the potential for further exploitation.

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