A Single Memristor-based TTL NOT logic

Una única lógica NOT TTL basada en Memristor

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Keywords

Memristor; NOT logic; TTL; hysteresis; green electronics; biodegradable electronics.

Abstract

This article presents a NOT logic gate circuit based on a single memristor, and analyzes it for different biological memristive samples based on extracted resistances. The simple resistor-voltage representation of the memristor in the logic circuit is used to formulate a methodology to tune the parameters of the circuit in accordance with TTL voltage values. The logic circuit consists of two resistors in series with the memristor. The input is connected to one end of the memristor, and the output is drawn across the series connection of the second resistor, and the memristor. The methodology comprises of two steps, where, in the first step, the logic 'low' TTL-input voltages are examined, and in the second step, the circuit is evaluated for logic 'high' TTL-input voltages. The methodology reveals that there is a mínimum voltage value of 'high' TTL-input beyond which the output does not fall within the logic 'low' TTL-output. The proposed technique may be extended to evaluate novel memristive materials for single memristor-based NOT logic.

Palabras clave

memristor; NO lógica; TTL; histéresis; electrónica verde; electrónica biodegradable.

Resumen

Este artículo presenta un circuito de puerta NO lógica basado en un solo memristor y lo analiza para diferentes muestras biológicas memristivas basadas en resistencias extraídas. La representación simple de voltaje de resistencia del memristor en el circuito lógico se usa para formular una metodología para ajustar los parámetros del circuito de acuerdo con los valores de voltaje TTL. El circuito lógico consta de dos resistencias en serie con el memristor. La entrada está conectada a un extremo del memristor y la salida se dibuja a través de la conexión en serie de la segunda resistencia y el memristor. La metodología consta de dos pasos, donde, en el primer paso, se examinan los voltajes de entrada TTL "bajos" lógicos, y en el segundo paso, se evalúa el circuito para voltajes de entrada TTL "altos" lógicos. La metodología revela que hay un valor de voltaje mínimo de entrada TTL "alta" más allá del cual la salida no cae dentro de la salida TTL lógica "baja". La técnica propuesta puede extenderse para evaluar nuevos materiales memristivos para la lógica NOT basada en un solo memristor.

Introduction

Leon Chua's proposal of the fourth passive element, the memristor, relates flux, and charge [1]. Since the inception of the TiO2 based memristor in 2008, the possibilities of exploration of memristors, and their applications have increased [2]. To realize such applications, the implementation of memristor-based digital logic circuits in TTL/ CMOS compatible style has always been essential. As of now, IMPLY, and MAGIC style of logic designs have been proposed, which, as opposed to TTL/ CMOS-based operation, are sequential in nature [3][4]. Memristive action has also been reported in biological materials like sweat ducts, Venus flytrap plant, and amoeba [1]. Biomaterial-based memristors have the potential to contribute to next-generation flexible, and green electronics.

This article proposes the concept of a NOT logic gate using a resistor-bias model of a single memristor compatible with TTL mode of operation. The logic based on TTL votages is applied to a number of reported biological memristors which give pinched hysterics loop in V-I plane. The

high off-state resistance, R_H, and low on-state resistance, R_L, are extracted from V-I plots of the reported samples. A simple methodology is proposed for setting up the circuit parameters, and voltage range of operation as per TTL.

Methodology

The proposed memristor-based NOT logic circuit is shown in Fig. 1 (a). The circuit consists of two resistors, R_1 and R_2 , connected in series with the memristor. The memristor resistance is represented as R_M. The input voltage, V_{IN}, corresponding to logic '0' or logic '1' is applied to one terminal of the memristor, and the other terminal is connected to the resistor, R_2. The output voltage, V_{OUT}, is taken across the series connection of R_2, and R_M as depicted in Fig. 1 (a). Depending on the input, R_M changes. If V_{IN} = '1', $R_M = R_L$, and if V_{IN} = '0', $R_M = R_H$, where, R_H, and R_L are high, and low resistances in off-state, and on-state respectively.

The methodology for tuning the circuit parameters as carried out on LTspice XVII is shown in Fig. 1 (b). The output voltage is given by $V_{OUT} = (V_{CC} - V_{IN})(R_2 + R_M) \Big/ (R_1 + R_2 + R_M)$. If $m = \frac{R_1}{R_2 + R_M}$, such that $R_1 = R_2$, we arrive at the relationship $R_1 = R_2 = \frac{m}{1-m} R_M$.

Results

Step I

For 10 biological memristors from literature as listed in Table I, taking m = 0.01, R_1, and R_2 are calculated, and considered in the circuit where a sweep of V_{IN} is done from 0 V – 0.8 V, having $R_M = R_H$, and V_{OUT} is plotted in Fig. 1 (c). It is observed that the values lie well within the TTL logic '1' range of 2 V – 5 V, and closer to 5 V for the range of TTL V_{IN}. The plots for all samples are exactly same because considering the conditions, we arrive at $V_{OUT} = V_H = \frac{(V_{CC} - V_L)(n+1)}{(2n+1)}$, where $n = \frac{m}{1-m}$ is a constant.

Step II

Carrying forward R_1, and R_2 as obtained from the previous step, a sweep of V_{IN} is done from 2 V – 5 V, having $R_M = R_L$, and V_{OUT} is plotted in Fig. 2 (a). In this case, $V_{OUT} = V_L = \frac{(V_{CC} - V_H)(nr+1)}{(2nr+1)}$, where, $r = R_H / R_L$. Since R_1, and R_2 are dependent on R_H, therefore, some values of V_{OUT} may lie outside the TTL logic '0' voltages corresponding to 0 V – 0.8 V. This further indicates that there is supposed to be a minimum value of $V_{IN} = V_{H,min}$ for which $V_{OUT} = V_L$ lies in the TTL logic '0' range. This is indicated by a shaded region in Fig. 2 (a), and listed in Table I.

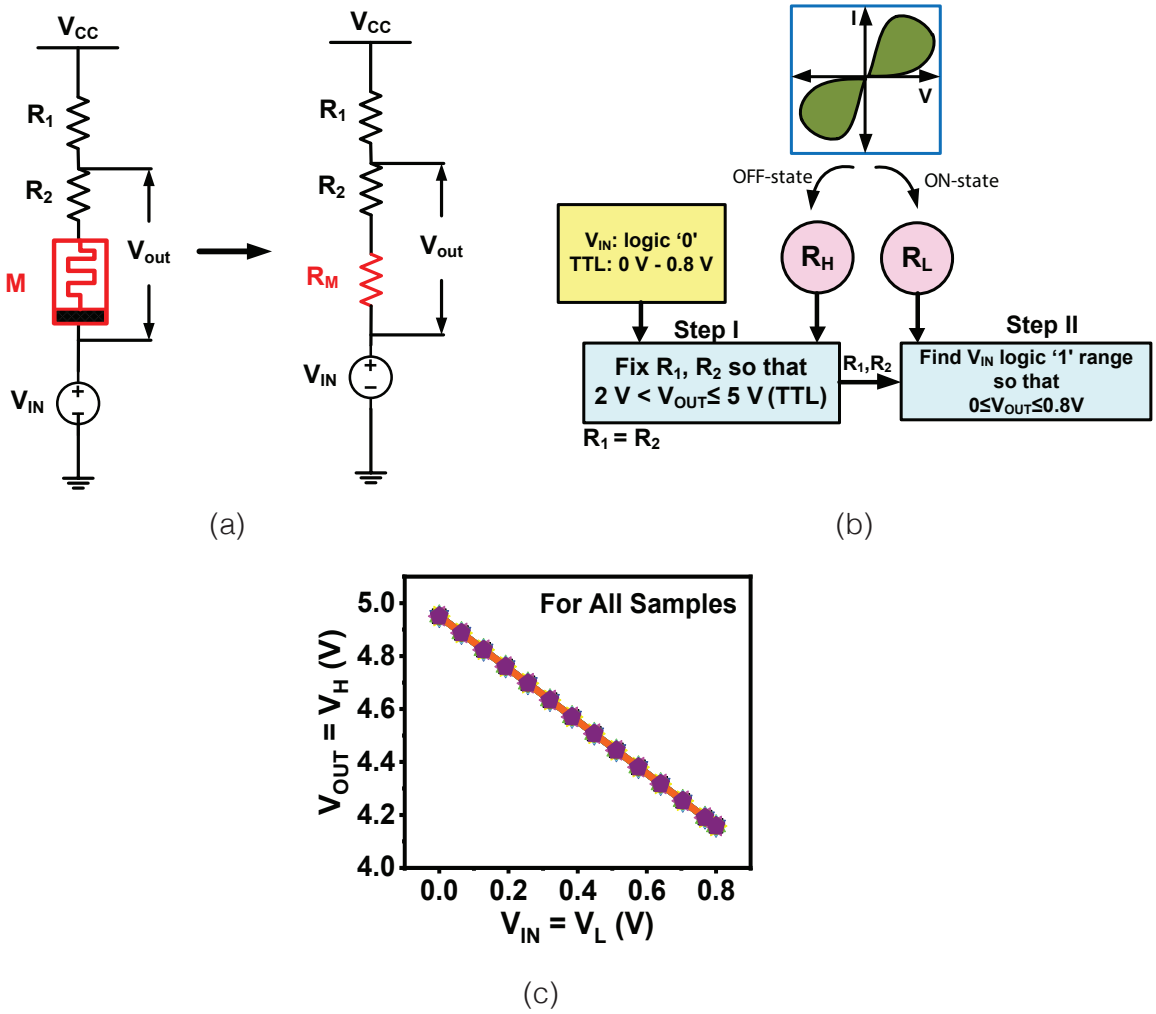

Figure 1. (a) NOT logic circuit using memristor polarity; (b) Flowchart showing the methodology; (c) $V_{OUT} = V_H$ versus $V_{IN} = V_L$ plot

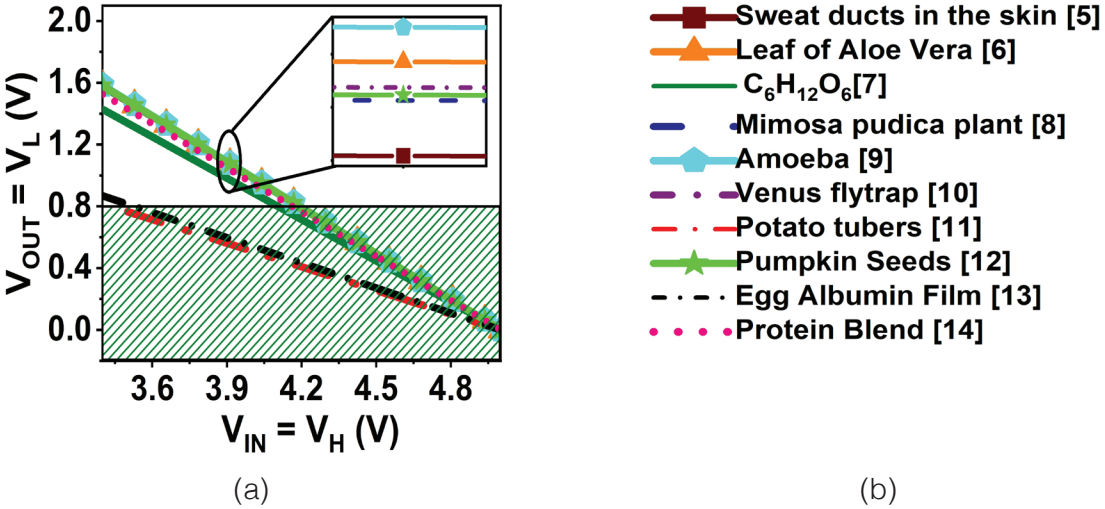

Figure 2. (a) $V_{OUT} = V_L$ versus $V_{IN} = V_H$ plot showing the valid TTL $V_{OUT} = V_L$ limit; (b) Legend for (a)

Table 1. Table for TTL Logic Showing R_H, R_L, r, R_1, R_2, $V_{H,min}$

Sl. No.	Memristor TTL NOT Logic Parameters				
	$R_H(k\Omega)$	$R_L(k\Omega)$	$r = R_H/R_L$	$R_1 = R_2$	$V_{IN} = V_{H,min}(V)$
[5]	417	360	1.15	4.21 kΩ	4.19
[6]	321	218	1.47	3.24kΩ	4.18
[7]	1.96	0.14516	13.5	19.79 Ω	4.10
[8]	108	88	1.22	1.09 kΩ	4.19
[9]	16	14	1.14	161Ω	4.19
[10]	73	69	1.05	737.3Ω	4.19
[11]	6060	2042	2.98	61.5kΩ	4.17
[12]	419	393	1.06	4.2kΩ	4.19
[13]	31.8	0.06	530	321Ω	3.52
[14]	1.112	0.4	2.78	11.23Ω	4.17

Conclusions

This work presented a simple circuit to implement a NOT logic gate by using a single memristor, and differential output. Considering 10 biological sample from literature, the conclusions of this article can be summed up as follows.

- The fixed resistors in the circuit, R_1 and R_2, which are equal, and proportional to R_H, were fixed by taking a value of m for logic '0' TTL input. In this article, m = 0.01 was considered.
- The resistors, R_1 and R_2, once fixed, were considered for logic '1' TTL input corresponding to which, the entire logic '0' TTL output was achieved for all samples.
- The same approach may be used for CMOS logic.

Acknowledgement

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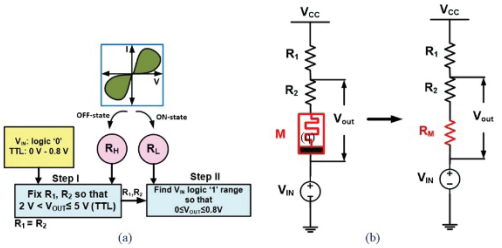

Fig. 1 (a) Flowchart showing the methodology; **(b)** NOT logic circuit using memristor polarity; **(c)** $V_{OUT} = V_H$ versus $V_{IN} = V_L$ plot

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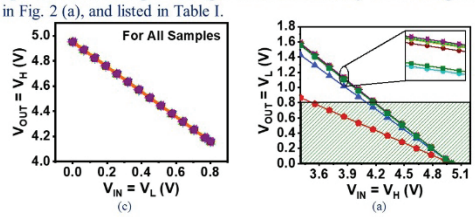

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